Design and Analysis of a Novel Quantum-MOS Sense Amplifier Circuit

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Abstract

A novel quantum-MOS sense amplifier circuit consisting of resonant tunneling diodes (RTD's) as pull-up devices and NMOS transistors is discussed in this paper. Compared to the conventional sense amplifier circuits using CMOS technology, the proposed QMOS sense amplifier exhibits about 20% higher sensing speed. The cross-coupled QMOS latch, which is at the heart of the sense amplifier circuit, has metastable and unstable states which are closely related to the I-V characteristics of the RTD's. The stability analysis has been made by using phase-plot diagram and how RTD parameters relate to circuit speed and robustness of the sense amplifier has been discussed.

1 Introduction

Design of the sense amplifier is one of the most critical and difficult tasks in a MOS implementation of high-density, high-speed dynamic random access memory (DRAM) chip. In conventional DRAMs, the sense amplifier circuit usually consists of a cross-coupled complementary MOS inverter pair (latch) since it has several merits including increased chip reliability, higher speed, lower transient power dissipation, and reduced voltage bounce noise, in comparison with purely n-type FET based sense amplifiers [1]. But the main drawback of a CMOS sense amplifier is its large area owing to bulky p-type MOS transistors and this poses a severe challenge in modern high-density DRAMs with low inter-cellar pitch width (about 3 λ). Optimization of the size of PMOS devices can only be accomplished at the cost of sensing speed and noise performance. Also, larger PMOS transistors tend to increase the bit-line RC delays due to increasing bit-line lengths. It is not entirely clear whether a good compromise between disparate conflicting requirements in the design of a sense amplifier can be achieved using the conventional CMOS technology. This paper introduces a new quantum-MOS technology (QMOS) and it shows how a good sense amplifier design can be made using QMOS circuits that do away with bulky PMOS transistors. QMOS technology co-integrates quantum devices such as the resonant tunneling diodes (RTD's) and NMOS transistors. This emerging technology has a large potential and may define the future of very large scale integrated (VLSI) circuits with faster speed as well as lower dynamic power dissipation as compared to the conventional CMOS circuits [2]. Wagt, *et. al.* has proposed a revolutionizing DRAM cell design that employs a pair of RTDs to store the cell information, and thereby decreases the effect of charge leakage in the storage capacitor, which, in turn, has been shown to decrease the power consumption of a DRAM chip by over one thousand times due to the elimination of cell refreshing [3]. In this paper, a novel RTD-based sense amplifier circuit, called a quantum MOS (QMOS) sense amplifier, is proposed and its operation is analyzed and verified through SPICE simulation. The goal of this work is to demonstrate how RTDs can make a great impact in the design and growth of future DRAM chips that will consume less power and will have improved memory cycle due to the co-integration of RTDs in memory array storage cells and also in sense amplifiers.

2 Operation Principle

Figure 1(a) shows a conventional cross-coupled CMOS inverter latch. The bit lines are precharged to half-V_{DD} since the CMOS inverter exhibits a high gain in its transient region. In the *READ* operation, the charge sharing between the bit line and the accessed cell induces a small voltage difference between BIT and $\overline{BIT}$ nodes. Once the voltage difference is established, the control signals, SE and $\overline{SE}$, activate the cross-coupled latch, and the small voltage difference is amplified to push the BIT voltage to either V_{DD}

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or 0, depending on the sign of initial voltage difference.

Figure 1(b) shows the proposed QMOS sense amplifier circuit. The CMOS inverter is replaced by the QMOS inverter that consists of an NMOS driver and an RTD load. As in the CMOS circuit, once the voltage difference between BIT and $\overline{BIT}$ nodes is built, the QMOS sense amplifier is enabled by the switching transistors, $M5 - M8$. Because of the higher current drive capability of the RTD load compared to the PMOS transistor, the QMOS sense amplifier is expected to have a faster sensing time.

3 Simulation Results

Figures 2 and 3 show a load line diagram of QMOS inverter, and a SPICE simulation result of sensing time of the coupled QMOS inverter, respectively. The circuit equation of Fig. 1(b) is given by,

$$C_B \frac{dv_1}{dt} = I_{RTD}(V_{DD} - v_1) - I_{TR}(v_2, v_1) \quad (1)$$

$$C_B \frac{dv_2}{dt} = I_{RTD}(V_{DD} - v_2) - I_{TR}(v_1, v_2) \quad (2)$$

where C_B is the bit-line capacitance, v_1 and v_2 are BIT and $\overline{BIT}$ voltages. The $I_{RTD}(v)$ and $I_{TR}(v_g, v_{ds})$ indicate the current-voltage characteristics of the RTD and NMOS transistor, respectively, which are given by,

$$I_{RTD}(v) = \begin{cases} \frac{I_P}{V_P} v & (0 \le v < V_P) \\ I_P - \frac{I_P - I_V}{V_V - V_P}(v - V_P) & (V_P \le v < V_V) \\ I_V + \frac{I_P - I_V}{V_{SEC} - V_V}(v - V_V) & (V_V \le v) \end{cases} \quad (3)$$

and

$$I_{TR}(v_g, v_{ds}) = \begin{cases} 0 & (v_g < V_T) \\ \beta[(v_g - V_T)v_{ds} - v_{ds}^2/2] & (v_{ds} < v_g - V_T) \\ \frac{\beta}{2}(v_g - V_T)^2 & (v_{ds} \ge v_g - V_T) \end{cases} \quad (4)$$

where the I_P, V_P, I_V, V_V, and V_{SEC} represent a peak current, a peak voltage, a valley current, a valley voltage and a second peak voltage for the RTD characteristics, respectively. The β and V_T are gain and threshold voltage, respectively, for the NMOS transistor. The RTDs with $I_P = 718\mu$A, $V_P = 0.8$V, $I_V = 77.4\mu$A, $V_V = 1.92$V, and $V_{SEC} = \infty$, and the transistors with $\beta = 2.0 \times 10^{-4}$A/V^2 and $V_T = 0.72$, are used in the proposed design. The initial value of the bitline voltage is 1.8 V and 1.7 V, and its capacitance is assumed to be 0.5 pF.

The dashed line in Fig. 3 indicates the sensing time of CMOS sense amplifier shown for the comparison. The NMOS characteristics are assumed to be the same in the both sense amplifier circuits. The PMOS characteristics of the CMOS sense amplifier is assumed to be symmetric to the NMOS characteristics($\beta_P = \beta_N$, $V_{TP} = -V_{TN}$). The sensing time, defined as a time at which both conditions $v_1 > 0.9V_{DD}$ and $v_2 < 0.1V_{DD}$ are simultaneously satisfied, is about 20% faster than that of the CMOS. This is due to the larger current drive capability of the RTD load than the PMOS. As the current drive capability of the pull-up load is larger, the charging time of the bitline capacitance becomes shorter. This fast charging time induces the reduction of discharging time of other bitline capacitance also, because the NMOS transistor of the discharging circuit quickly turns on due to the cross coupled connection.

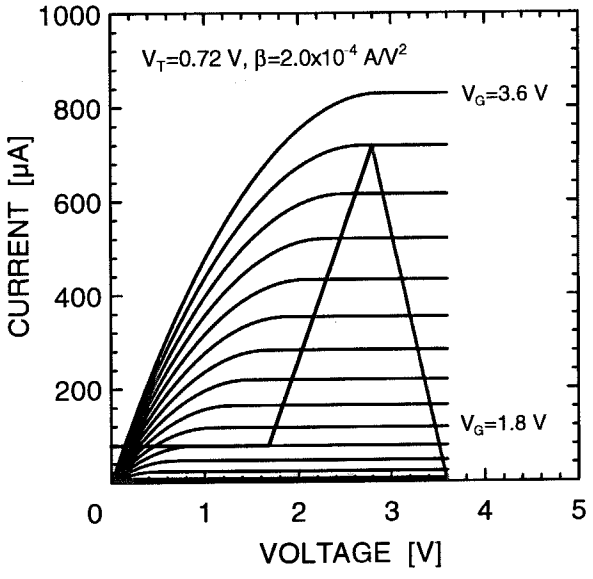

Figure 2. Load line diagram for QMOS inverter circuit

4 Stability Analysis

In this section, the stability of the solution of Eqs. 1 and 2 for a given initial condition is discussed by using phase diagram. Figure 4 shows voltage transfer characteristics (VTC) of each inverter. The solid and dashed VTC lines indicate the solution for $dv_2/dt = 0$ and $dv_1/dt = 0$, respectively. The intersection points, therefore, represent the equilibrium points of Eqs. 1 and 2. Unlike the CMOS sense amplifier, the QMOS sense amplifier circuit has three stable points (A, B, and C), one meta-stable point (D), and one unstable point (E), due to its Z-shaped VTC, as shown in Fig. 4. The dotted lines in Fig. 4(b) indicate the trajectory curves of Eqs. 1 and 2 for different initial condi-

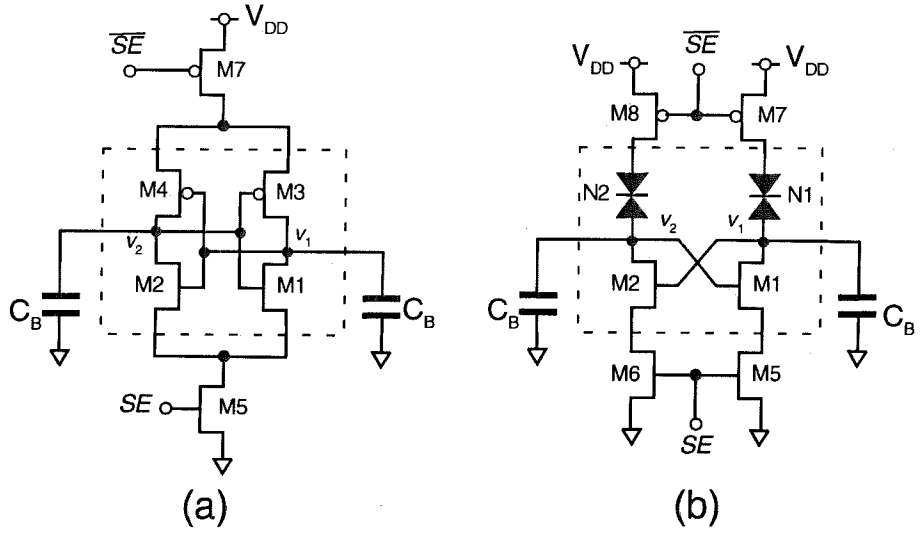

Figure 1. Sense amplifier circuit. (a) CMOS, (b) QMOS

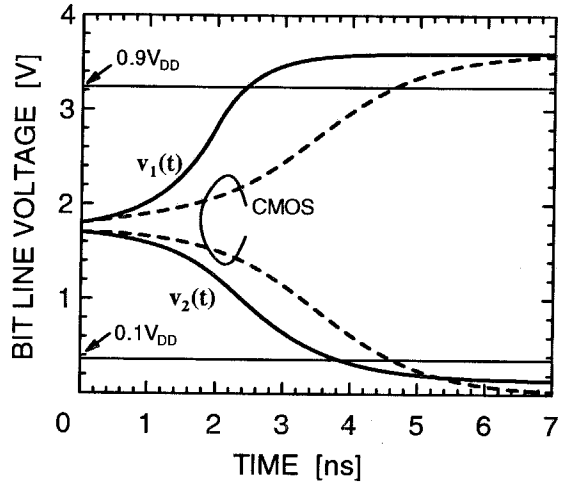

Figure 3. Simulation results for QMOS and CMOS sense amplifier circuit

tions. From the point $P_1(1.8, 1.7)$, where $dv_1/dt > 0$ and $dv_2/dt < 0$, the solution directly goes to the stable point B (Fig. 3). From $P_2(2.0, 1.9)$ or $P_3(2.4, 2.3)$, where both dv_1/dt, and dv_2/dt, > 0, the trajectory once goes upward, and when it reaches to the solid VTC curve, it turns to the downward, resulting in going to the point B. When it starts from the point $P_4(2.5, 2.4)$, however, the solution reaches to the dashed VTC curve, resulting in convergence to the point C, which is an erroneous operation of the sense amplifier.

This erroneous behavior can be controlled by optimizing the RTD parameters. If the point F on the solid VTC curve, corresponding to the peak position of RTD characteristics, is moved closer to the line of $v_2 = v_1$, the instability is reduced. The v_1 and v_2 value at point F, which is determined by the peak current and voltage of the RTD characteristics, is given by,

$$\begin{aligned} v_1|_F &= V_T + \sqrt{\frac{2I_P}{\beta}} \\ v_2|_F &= V_{DD} - V_P \end{aligned} \tag{5}$$

From the above equations, when I_P is decreased, the point F is moved to left. When V_P is decreased, on the other hand, the point F is moved upward. Therefore, the decrease of I_P and/or V_P can reduce the instability. Figure 5 shows an initial condition dependence of the sensing time for three different peak voltage values (V_P =0.8, 0.6, and 0.4V). The initial condition for $v_1(t)$ and $v_2(t)$ are assumed to be,

$$\begin{aligned} v_1(0) &= 1.9 + \Delta v \\ v_2(0) &= v_1(0) - 0.1 \end{aligned} \tag{6}$$

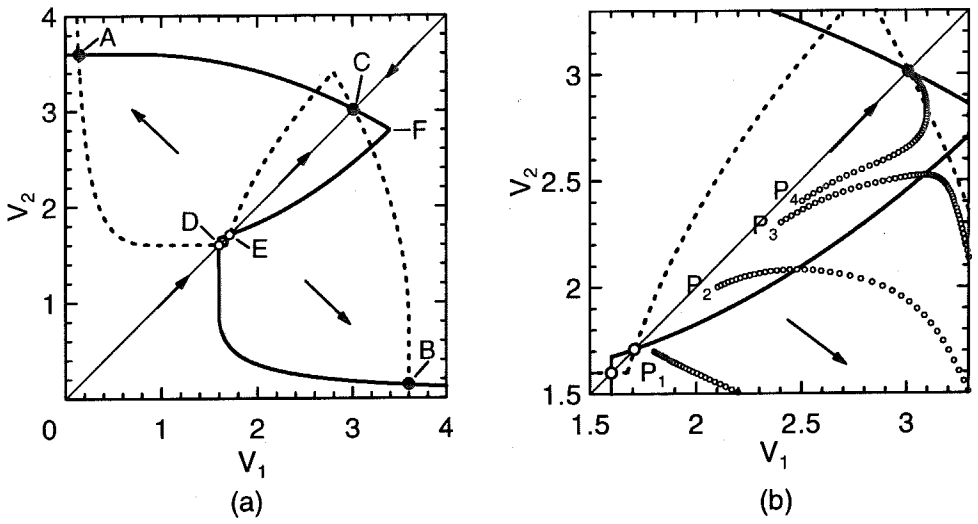

Figure 4. Voltage transfer characteristics of QMOS inverter pair

where Δv indicates the voltage fluctuation during the bitline precharge cycle. As shown in Fig. 4 (b), when Δv equals to 0.5V at $V_P = 0.8$V, which corresponds to the point P_4 in Fig. 4 (b), the sensing time becomes infinity due to the erroneous operation. Figure 5 indicates that the reduction of V_P can increase the normal operation margin against the initial voltage fluctuation without degrading the sensing speed.

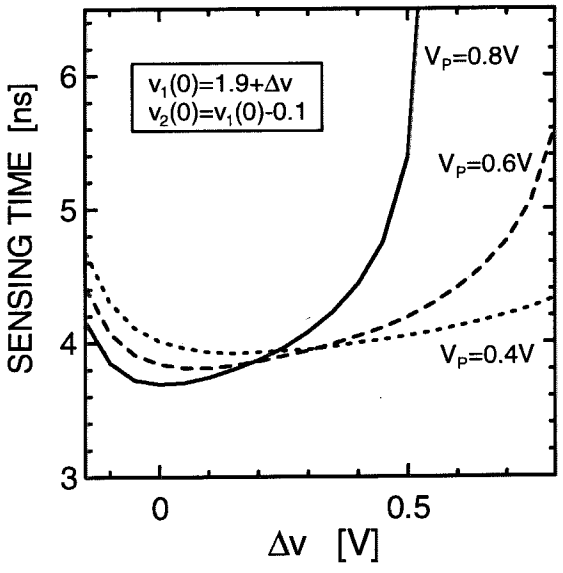

Figure 5. Initial voltage fluctuation dependence of the sensing time

5 Conclusion

Design of a novel QMOS sense amplifier circuit consisting of RTD pull-up loads and NMOS transistors is discussed in this paper and its operation is analyzed. Compared to the conventional CMOS sense amplifier, the QMOS design exhibits about 20% higher sensing speed due to the larger current drive capability of the RTD load. The instability against the initial condition has been analyzed by drawing phase plot diagram. It has been found that by reducing the peak current and/or peak voltage of the RTD circuit instability can be tackled.

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