

Self-Assembly Based Approaches for Metal/Molecule/Semiconductor Nanoelectronic Circuits

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Abstract

This paper describes a technological approach which combines the nanoscale elements available from molecular devices and self-assembled molecular/nanoparticle systems with semiconductor devices which can provide the gain or bistability required for computational functionality. The architectural motivation for these configurations and experimental demonstrations of several key technologies for this hybrid approach are described.

1. Introduction

Recent theoretical and experimental studies have established that both discrete molecular devices and self-assembled systems comprised of molecular wires and metal nanoparticles can be realized and characterized. The related studies have already led to fundamental advances concerning the electronic properties of these nanoscale devices/systems (e.g., mechanisms for electron transport in individual molecules as well as larger molecular/nanoparticle systems). While these advances are significant from a scientific perspective, from a computational and systems perspective, they can best be regarded as a collective first step toward a technology for future realizations of nanoelectronic circuits. The realization of nanoelectronic circuits based solely on self-assembled molecular and/or nano-cluster systems would require the development of a complex technology, including active devices, nodes, interconnects and mechanisms for power distribution and dissipation, that parallels the current-day semiconductor technology. While these capabilities are, in principle, possible, the number of significant challenges indicates that a somewhat different approach might be required

in order to begin using these capabilities in nanoelectronic circuits. In particular, it should be possible to realize nanoelectronic circuits sooner by utilizing the inherent nanoscale features of these systems along with well-established semiconductor technology.

This paper describes a technological approach which combines the nanoscale elements available from molecular devices and self-assembled molecular/nanoparticle systems with semiconductor devices which can provide the gain or bistability required for computational functionality. The hybrid approach presented here could be used to realize a nanoscale computational circuit. Such a marriage could exploit directed self-assembly techniques, which are suitable for realizing nanometer scale elements, and semiconductor devices, which can provide the basic functionality required for realizing a logic or memory cell, to design robust high density circuits. In particular, this paper focuses on the experimental progress made toward developing the components required for this circuit topology and discuss the prospects and challenges for further development.

2. Architectural Motivation

In previous theoretical papers [1-2], a computational architecture has been proposed, based on the desire to perform computational functions using structures and interconnections with minimal complexity, as might be realized by self-assembly techniques. The proposed architecture utilizes locally interconnected cells of computational nodes, with the nodes arranged in 2-D arrays. This overall structure, well defined cells composed of 2-D arrays of nanoscale nodes, can be realized using directed self-assembly techniques, as will be described later. In order to provide an active device functionality, each metallic node within a computational

cell is coupled to a semiconductor mesa with nonlinear, nonmonotone I-V relationship (e.g. a resonant tunneling diode (RTD) device with an "N"-shaped I-V curve). The logic state of each node corresponds to the node voltage; a bias connection to each node/mesa provides a quasi-constant current to latch the RTD device (and therefore the node) into a high or low voltage state. While the two-terminal devices (diodes) do not have the 3-terminal gain associated with transistors, the bistable latching provides suitable functionality for robust, room-temperature computational circuits.

Local resistive interconnects (nearest neighbor) are sufficient to provide computational functions such as associative memory. Boolean logic functions can also be realized using diode coupling between cells and clocking of bias voltages to provide directionality and specific logic functionalities. Although bias connections are required for each element, the I/O connections can be at the edge of the circuit. Such topologies can display a wide range of functionalities (of which Boolean logic is the most basic), can operate at room temperature and can be scaled to nanometer dimensions without loss of functionality, provided that suitable components are available.

3. Demonstration of Key Technologies

Several enabling technologies have been developed for the key components required to realize comparable circuits at the nanoscale level. These developments are aimed at providing self-assembly based fabrication techniques which are suitable for development of nanoelectronic circuits and which can potentially provide high-throughput, low-cost fabrication of high density circuit components. In addition, it is necessary to employ semiconductor device structures and contact interfaces which are suitable for use with the self-assembly fabrication and which are scaleable to nanometer dimensions. A key challenge is to develop fabrication techniques which can provide the uniform nanoscale components characteristic of self-assembly techniques along with a compatible lithography-based patterning technique for definition of cells (consisting of multiple nanoscale nodes) and specific nearest-neighbor interconnects.

In previous reports, we have described self-assembly synthesis techniques which can provide highly ordered arrays of islands at the nanometer scale. High quality linked cluster networks (LCNs), consisting of close-packed 2-D arrays of 4 nm diameter metal clusters, have been demonstrated [3]. In the LCN structures, the intercluster resistance can be controlled by choice of the conjugated organic molecules which link adja-

cent clusters. The LCN technology can provide high density node arrays with controllable resistive local interconnections.

We have also developed and characterized semiconductor heterostructures which provide chemically stable surfaces and low-resistance nonalloyed ohmic contact interfaces [4-7], both essential for semiconductor based devices which exploit chemical self-assembly for a significant portion of the device definition. These capabilities have been utilized to demonstrate resonant tunneling devices with very shallow active layers, which allows device isolation without deep etching in order to maintain nearly planar surfaces. Scaling of devices such as resonant tunneling diodes to cross-sectional areas of 5-50 nm will require advances in areas such as ohmic contact technology, surface passivation and device patterning. The use of shallow devices with nonalloyed contacts will be required in order for the process to be compatible with chemical self-assembly techniques, which generally require near planarity of the surface and low temperature processing. In order to prevent surface depletion from pinching off the device mesa, appropriate surface passivation layers and patterning by shallow etching will also be required.

Recent developments have been aimed at merging chemical self-assembly based nanotechnology with semiconductor device technology in order to provide nanometer scale active devices, patterned array of metallic nodes, and appropriate nanoscale interconnect elements. We have demonstrated the definition of 20 nm semiconductor mesas using a Au nanocluster as an in-situ etching mask. We have applied the nonalloyed ohmic contact technology to the development of low-resistance nanocontacts to n-type GaAs devices. Using Au nanoclusters as the contact metal regions, we have fabricated and characterized contacts with a well-controlled area of 10 square nanometers ($1 \times 10^{-13} \text{cm}^2$). This contact structure has a specific contact resistance of $1 \times 10^{-6} \Omega \text{cm}^2$ and can pass a current density of $1 \times 10^6 \text{A/cm}^2$, both comparable to the performance of high quality large area contacts to n-type GaAs.

Conventional self-assembly techniques can provide relatively uniform arrays of dots or lines, but generally do not provide the specific configurations required for sophisticated circuits. In contrast, we have demonstrated "directed self-assembly" techniques in which high quality 2-D arrays of nanoscale metallic clusters can be formed in selected regions on a semiconductor substrate. The resulting structure provides the nanocluster arrays exclusively within regions defined by a lithographic technique, thus providing a means to realize desired structures such as cells and intracell re-

gions while still utilizing self-assembly for high density node elements. This approach utilizes patterned organic monolayers on the semiconductor substrate as selective tether regions for metallic clusters. Since these techniques work on semiconductor substrates, they are compatible with the developments needed for experimental realization of the architectural configurations described earlier. Scanning tunneling microscopy (STM) techniques have been used to image the close-packed arrays of nanoclusters and to characterize the electrical conduction between the nanoclusters and the semiconductor substrate. A representative STM image of a close-packed array of 4 nm diameter Au clusters is shown in Fig. 1. The resulting structures can provide the well-defined computational nodes required for the architecture described earlier. In addition, this technology can be used to realize "molecular ribbons", i.e. interconnect lines consisting of metallic nanoclusters linked by conducting organic molecules [8]. The molecular ribbons could be used as interconnect lines in semiconductor or related nanoelectronic circuits. They can provide low-resistance lines which combine the structural and electronic flexibility of molecular components [9] with the stability and conductivity of metallic lines. Since they are formed by directed self-assembly, they can in principle be formed into desired patterns without the use of high resolution lithography. As has been shown in this study, these ribbon structures can provide low-resistance interfaces to semiconductor devices as well as other structures.

4. Conclusion

The components described in this work provide a basic set of building blocks to realize nanometer scale circuit elements incorporating metallic nodes, semiconductor mesas and molecular-based interconnects. The focus of the current work is to integrate the nanoscale devices and interconnect components into unit cells, and eventually complete computational cells. As a proof of concept, we have recently demonstrated and electrically characterized a 4 nm "unit cell" consisting of a 4 nm diameter Au cluster mechanically and electrically coupled to GaAs-based RTD device layer via conjugated organic molecules.

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Figure 1. A 43 nm × 43 nm STM topographic image of a close-packed array of 4 nm Au clusters tethered on a GaAs device layer. Image is acquired with a tunneling current of 200 pA and a sample bias voltage of -1.5 V.

6. References

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