Design For Testability Method for CML Digital Circuits

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Abstract

This paper presents a new Design for Testability (DFT) technique for Current-Mode Logic (CML) circuits. This new technique, with little overhead, using built-in detectors, monitors all gate output swings and flags all abnormal voltage excursions. These detectors cover classes of faults that cannot be tested by stuck-at testing methods only. Circuit simulations have shown that abnormal gate output excursions caused by the presence of a defect are common with CML. We also show that this technique works well below "at-speed" frequencies. Finally, variants of the built-in detectors with reduced area overhead are proposed.

1. Introduction

As technology improves with time, some design techniques such as ECL and CML, once set aside, are now reconsidered. Due to that technological evolution, device area has decreased significantly and dynamic power dissipation has been reduced with the size of transistors. For instance, the circuits reported in [1] lead to gate delays far below 1 ns and bit rates of up to 50 Gbits/s. ECL/CML bipolar technologies have an edge over CMOS when speed is the main concern. For example, architectures of Gbits/s transceivers [2] are implemented in two level CML and ECL circuits.

Considering the growing popularity of CML circuits, their testability should be assessed carefully. A quick look at the literature shows that ECL/CML testability has not been thoroughly studied. It appears that due to their market dominance, MOS technologies have attracted most of the attention of the industrial and scientific community. However, some recent works on ECL/CML testability have shown that these circuits have unique fault sensitivities, and that classical stuck-at faults is far from providing sufficient defect coverage[3][4][5][6]. Furthermore, it was shown that ECL combinational gate chains have a tendency to heal back from faults in the first stages [5]. Frequently reported faults are line stuck-at [3][7], truth-table [3], like [4], wired-OR [8], byzantine [5], reduced noise-margin [3][5], undefined logic-level [6][8], delay [3][6], feedback oscillation [8], sequential behaviour [8] and I_{ddq} [3]. The probable manufacturing defects causing these faults are interconnect and resistor shorts or opens, piped transistors, bridges (wires making contact) and broken lines [3][4][6].

To deal with the observed variety of faults, design for testability methods of several flavours were proposed. For instance, a simple technique to test for like-faults in ECL was devised by Menon [4]. The proposed technique uses a standard XOR gate to verify the complementary behaviour of the gate outputs. This technique introduces a very high area overhead (one test gate for every circuit gate). Delay measurement techniques have been developed to test ECL-CMOS RAM macros [9]. Using ECL flip-flops on the inputs and outputs of the CMOS RAM macros and using a pattern generator to stimulate the memories, Higeta et al. measured the path delay within the macros in test clock cycles. This technique may be useful for CML circuits, however it cannot fully test for even obvious delay faults. Considering that each gate can have a modest variation in delay of 10% of nominal value, the tester evaluating a 10 gate deep chain could escape a faulty gate going twice slower than nominal, when all others have their nominal delay value. Also, an at-speed built-in self-test (BIST) circuit was proposed by Jorczyk et al. [10] to test ECL integrated circuits, and it was shown that it yields a better defect detection than slow speed test. However, this technique requires significant design efforts and high area overhead.

To deal with the problem of reduced noise-margins and of fault symptoms healing, Anderson [5] presents a patented technique (from IBM) that would stress a circuit enough to make the recovery impossible, forcing the fault to appear as stuck-at. This technique uses two additional power lines in test mode to bias the differential stage of all gates one way or the other. Small devices are added to each gate to isolate the circuit from the additional lines in normal mode and to protect the circuit from unwanted noise and loading. A second technique proposed and patented by Cecchi and Delbert [11] was oriented toward a specific fault that could not be observed easily. The cause of the fault had been pinpointed to a probable defect related to the contact layer. Through modification of the layout of standard cells, they were able to guarantee that any defect within this layer could only map into a stuck-at fault.

In this paper, we present novel design for testability techniques to detect faults in CML circuits [12]. We show that our technique is superior to prior art in detecting a defect class observed in CML circuits, without reverting to at speed test approaches.

In section 2 of this paper, we will first review the basic design principles in CML. Section 3 analyses possible defects in CML circuits and the fault model studied in this paper is presented in section 4. We then describe in section 5 the method we used to simulate the presence of a defect and its consequences. Section 6 proposes the techniques we developed for testing abnormal

amplitude excursions, and section 7 presents our main conclusions.

2. CML Basic Design Principles

CML is a circuit level design style well adapted to fast bipolar digital circuit libraries. It is based upon a simple differential amplifier as shown in Figure 1. The amplifier is supplied with a stable current provided by transistor Q3. To stabilize this current, an environment independent voltage generator feeds the base of transistor Q3 with a fixed bias voltage. The power of this design comes from its functional simplicity. Transistors Q1 and Q2 steer the steady current through one of the two branches by turning on one transistor or the other with input signals *a* and *ab*. The current in the selected branch will create a voltage drop across its resistor, while in the other branch, where no current flows, the output voltage is kept to *vgnd*. The collectors of transistors Q1 and Q2 form a pair used as gate outputs (signals *op* and *opb*). In CML, each digital signal is thus represented by the voltage difference between two nodes, which increases the gate's noise margin. This differential signal is large enough to fully steer the current flowing in the gates it drives.

To implement more complex gates (e.g. AND, OR, MUX), vertical stacking of differential pairs is used. Stacked pairs are also used to steer the bias current to produce the desired function. To make sure the gate functions correctly, one must always make sure that the current has a path through a branch to vgnd. Due to the fixed power supply voltage, stacking is limited. To avoid forward-biased base to collector junctions of lower differential pairs, gate outputs must be level shifted by one VBE before driving them.

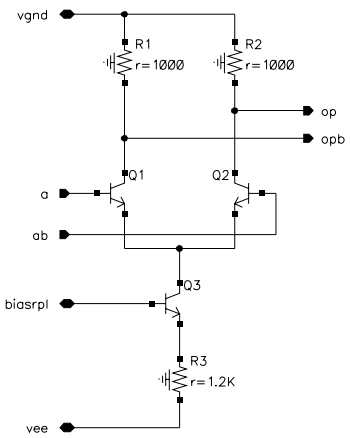


Figure 1 Basic CML Data Buffer (*vee* = 0 Vand *vgnd*=3.3 V)

Several advantages of CML logic families lie in suitable circuit design. High speed derives from non-saturated current steering and small voltage swings (~250 mV). Current steering limits *dI/dt* in the supply rails irrespective of circuit activity. Crosstalk is reduced due to paired differential signals, cancelling much of the independent magnetic fields they generate. A second notable advantage of using CML differential signals is the high signal to noise ratio, in spite of the small output signal swing. Also, small output swings provides a reduction in dynamic power consumption. Furthermore, CML gates always provide a signal and its complement, which simplifies circuits and reduces logical depth when inverted signals are needed.

3. Defects Encountered in CML Circuits

Throughout the literature, different defects encountered in bipolar processes have been exposed and some corresponding low level fault models were suggested. This section briefly reviews the most common types of defects.

Semiconductors manufacturing processes are subject to various imperfections and parametric variations that cause segments of layers to be connected together, a segment to be severed or a layer to have a thickness smaller than expected. For instance, if a layer is significantly thinner on a localized region, this region may fuse due to electromigration. If the current that flows through the layer is in the plane of the die, the segment of layer may end up severed. But, if the current flows in a direction orthogonal to the plane of the die, like in the case of a contact, one layer may be isolated, while current still flows between layer segments above or underneath.

Another class of defects is associated with bipolar devices. Bipolar transistors are characterized by a current gain which is determined by the base thickness. That thickness may be modulated by various phenomenon. For instance, the so-called dislocations of the active semiconductor layer are physical imperfections that can modulate the effective base thickness, when they fall in the base region. This generally creates a spot of very high gain and excessive leakage current, which is known as a collector to emitter pipe. Vertical transistors (usually NPN) are more prone to piping.

Severed segments, also called opens, are commonly found at transistor nodes, wires and resistor strips. Shorts are found as well between transistor nodes and resistors. Finally, bridges are resistive shorts between metal layers, 'bridging' two signals together.

The above defects can be modelled with good accuracy at the device level [3][6](e.g. transistor and resistor). Such models include shorts, bridges, opens or pipes. Thus, in a Spice-like simulator, a resistor of small value (~1 Ω) can be used to model shorts and bridges. To simulate an open, we can split a node and add a 100 MΩ resistor in parallel to a 1 fF capacitor to link the two parts together. The pipe is usually modelled by a resistor of a few KΩ between the collector and emitter of a transistor.

If the objective is to evaluate fault coverage accurately, the distributions of defect size and occurrence

probability in different layers are needed. Such information is usually unavailable, and it is thus common to treat defects as equiprobable.

4. Fault Models

Device level modelling is the most accurate way to simulate the effects of defects, but it is usually too complex, and accurate device level models of defective components are not available. Similarly, one could attempt to analyse all faults to uncover the defects that caused them, but that is impractical. A better way to deal with the problem is to identify the electrical consequences of defects within the circuit so that the results could be relayed to output pins when the chip is fully packaged. Such a model is called a fault model. Of course, to validate a list of probable faults, it is necessary to see it happen in a defective processed circuit.

Fault models found in the literature for ECL/CML circuits are numerous. As in CMOS, some defects produce stuck-at faults. Figure 2 shows the effect on a simple data buffer of a collector to emitter short on transistor Q2 (see Figure 1) causing an output stuck-at 0 fault. The input pair signals are named *af* and *abf* and the output pair signals are named *opf* and *opbf*.

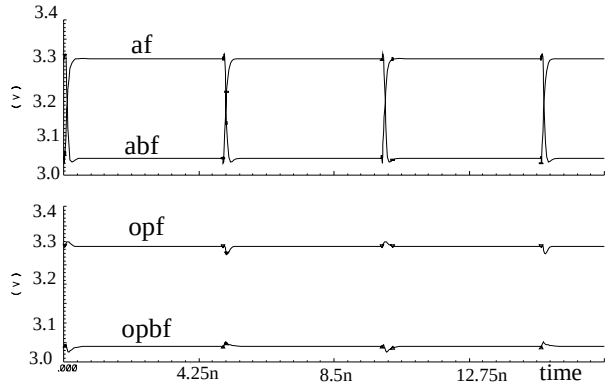


Figure 2 Typical stuck-at fault

Simulations have shown that several defects map into increased noise-margins, or more simply, produce a low logic voltage much lower than the standard V_{low}. Therefore, a testing technique to detect these faults is here proposed and should help to increase the fault coverage if combined with the detection of other fault models.

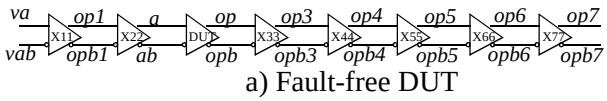
5. Defect Injection and Circuit Behaviour

In this work, the study of fault behaviour is based on realistic circuit level faults simulated with an analog circuit simulator (Spectretm^{TM}). The studied circuit level faults are: transistor pipes, transistor node opens, transistor node shorts, bridges, open in wires, resistor shorts and resistor opens.

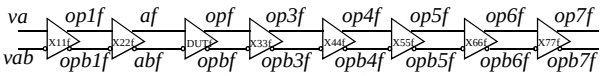
Results show that some defects can cause an output low voltage level to be much lower than the normal value. This paper focuses on this particular class of fault that in many cases, no other existing fault testing method would detect. In practice, the test bench used was a chain of buffers where the differential inputs of each gate are taken from the differential outputs of a preceding gate. It is of interest that in such a chain, the degraded output signals of a gate can be restored after few logic stages.

As a typical case of that phenomenon, we studied the fault masking problems associated with a current source transistor (Q3) collector-emitter (C-E) pipe on a standard CML buffer (Figure 1). The test circuit consists of a chain of 8 buffers (Figure 3). The device under test containing the defect is the third buffer.

Figure 4 shows the effect of a 4 KΩ pipe on Q3 (see Figure 1) on the outputs of the chain. It presents both the fault-free and faulty chains for the output signals of buffers DUT, DUTf, X66 and X66f, when the input signal oscillates at a frequency of 100 MHz. At the output of the faulty gate, the voltage swing has nearly doubled. But, after 4 logic gates, the degraded signal due to the pipe can be completely restored both in terms of logic levels and shape of a propagated transition.



a) Fault-free DUT



b) DUT with transistor pipe

Figure 3 Test circuit (buffer chain)

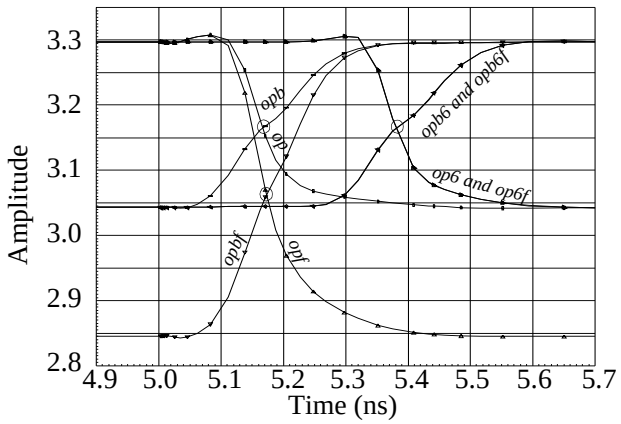


Figure 4 Third (*op* and *opb*) and sixth (*op6* and *opb6*) outputs with a 4 KΩ pipe

In a first attempt to detect such a fault, we evaluated its impact on gate delays, since the usual means of testing parametric faults is to test path delays. In Table 1, we give the measured propagation delays at different buffer outputs (input signal frequency: 100 MHz). These delays were measured when the output crosses 3.165 V, which is the normal crossing point of an output and its complement. This voltage reference would be representative of how ECL-type gates would convert the observed output voltage into logical values. From Table 1 we observe that the normal gate delay is 53 ps.

Also from Table 1, a delay twice the size of normal conditions can be observed on one of the outputs of the DUT (*opb*) while its complement (*op*) could be perceived as going faster than the fault-free signal. A remarkable result is the small difference in delay between the fault-free and faulty chain at the final output stage (*op6* and *opb6*). The result is remarkable because what may have seemed to be a delay testable fault at the DUTf, healed back to a difference which is insignificant after a few CML stages. That phenomenon was observed with several different defects in CML gates.

Table 1: Delay of different buffer outputs *vs* initial signal with a 4 KΩ pipe on Q3 of DUTf

	va *vab*	*op1* *op1b*	*a* *ab*	*op* *opb*	*op3* *opb3*	*op4* *opb4*	*op5* *opb5*	*op6* *opb6*
FF (ps)[a]	*0* *0*	*51* *64*	*105* *112*	*163* *163*	*216* *216*	*269* *269*	*322* *322*	*376* *376*
Pipe (ps)[b]	*0* *0*	*51* *64*	*113* *115*	*147* *221*	*219* *199*	*269* *272*	*324* *322*	*376* *376*
Δt *(ps)*[c]	*0* *0*	*0* *0*	*8* *3*	*-16* *58*	*3* *-17*	*0* *3*	*2* *0*	*0* *1*

a. FF: Delays measured on the fault-free chain
b. Pipe: Delays measured on the faulty chain containing a 4 KΩ C-E pipe
c. Δt: Difference in delays between the fault-free and faulty chains

To better understand the healing phenomenon, we repeated the delay measurements by using the actual crossing voltage, whatever its value, as the time measurement point. Using that delay measurement method, the results in Table 2 predict that even at DUTf, the delay differences were modest.

Table 2: Delay of different buffer outputs compared to the input signal *va*

	va	*op1*	*a*	*op*	*op3*	*op4*	*op5*	*op6*
τ_{FF}[a] *(ps)*	*0*	*56*	*110*	*163*	*216*	*269*	*321*	*375*
delay$_{FF}$ *(ps)*	--	*56*	*54*	*53*	*53*	*53*	*52*	*54*
τ_{Pipe}[b] *(ps)*	*0*	*56*	*114*	*170*	*217*	*270*	*323*	*376*
delay$_{Pipe}$ *(ps)*	--	*56*	*58*	*56*	*47*	*53*	*53*	*53*
$\Delta\tau_d$ *(ps)*	--	*0*	*4*	*7*	*1*	*1*	*2*	*1*
Δ*%*[c]	--	*0*	*7*	*13*	*2*	*2*	*4*	*2*

a. τ_{FF}: fault free
b. τ_{Pipe}: Q3 of DUTf with a 4 KΩ C-E pipe
c. $\Delta\tau_d$ compared to the gate's delay

Coming back to Figure 4, we already noticed that the main observable impact of the defect is an increase of the voltage swing. That swing was characterized over a wide range of pipe values and stimulation signal frequencies, and the corresponding output swings are reported in Figure 5 .

Note that as the pipe values get large, the levels come closer to their defect free values and this parametric disturbance becomes almost undetectable. The excessive amplitude of the low excursion also decreases with increasing frequency.

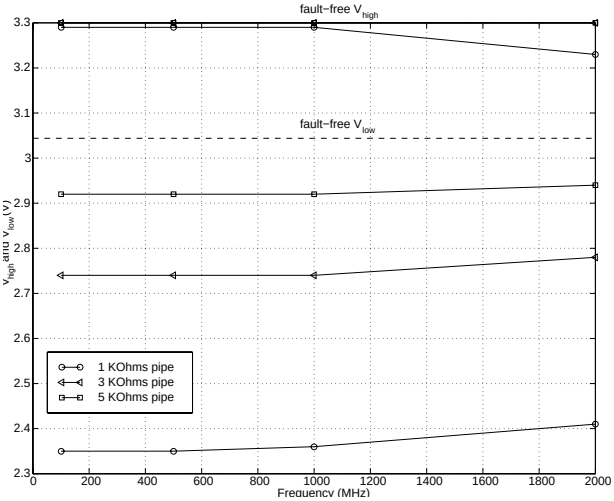


Figure 5 V_{low} and V_{high} vs. pipe value and frequency

6. Amplitude Testing

In order to detect excessive swings, a DFT technique has been developed. This technique uses non-intrusive built-in detectors implemented at the output of each gate to convert degraded signals into a logic value that reflects the presence of a fault. Two types of implementations have been proposed and then improved for a better stability.

6.1 Variant 1 - Single-Sided

The first type of built-in detector consists of a transistor with a diode (or resistor) - capacitor parallel load network. The detector is connected to outputs op and opb of each circuit cell (Figure 6). Based on circuit simulations, it was found that this detector only detects amplitudes greater than 0.57 V (equivalent to a 3 KΩ pipe on Q3, see Figure 6).

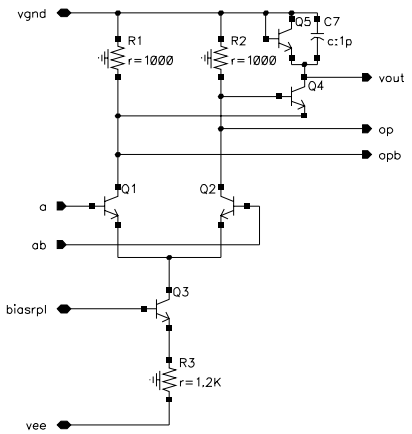


Figure 6 Proposed built-in detector (variant 1)

The actual test circuit is built of transistors Q4 and Q5

as well as capacitor C7. Whenever *opb* goes lower than *op* by more than 0.57 V, a current flows through transistor Q4 (from collector to emitter) sinking current from transistor Q5, connected as a diode, which acts as a non-linear resistor. This current builds a voltage difference between the diode's nodes, lowering *vout*. To help stabilize *vout* at a lower voltage than *vgnd*, capacitor C7 is used. In normal conditions, *opb* does not go lower than *op* by more than 0.57 V, and thus no current flows through Q4, keeping *vout* at *vgnd*. Since *vout* is lowered only when an amplitude fault is present, the signal can be compared to a reference voltage with a standard buffer (working as a comparator), transforming the degraded signal into a logic signal. Section 6.3 analyses the impact of such a comparator.

The detector output voltage was measured at different frequencies as a function of different combinations of load (Resistor, Capacitor) values, and of C-E pipe resistance values on Q3 (the current source transistor). The loads considered are diode-capacitor or resistor-capacitor combinations. As mentioned earlier, the diode is used as a non-linear resistance that offers a relatively high dynamic resistance at low currents, while offering a low dynamic resistance at high currents.

The detector output waveform is shown in Figure 7, when a (1 KΩ) collector-emitter pipe is present on transistor Q3 for a diode-capacitor (10 pF) load when input signal is 100 MHz. The waveform is characterized by a transient period and a relatively stable period. In that stable period, a ripple was observed with an amplitude that varies with loading and operating conditions. We define the time to stability ($\mathbf{t}_{stability}$) as the time where the signal reaches the first minimum value on the output voltage and V_{max} as the maximum voltage of the rippling signal on the detector when stability is reached.

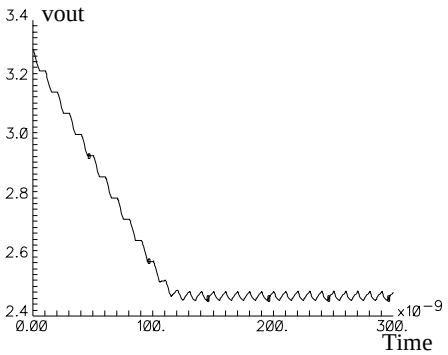


Figure 7 Response of the detector when 1 KΩ pipe and 10 pF load at 100 MHz

Figure 8 summarises the time to stability ($\mathbf{t}_{stability}$) according to frequency, pipe value and load capacitor value. Good results were also obtained by replacing the Q5 transistor with a 160 KΩ resistor. Note that the time to obtain a stable output voltage ($\mathbf{t}_{stability}$) increases significantly with frequency. This time can be much longer with a resistor–capacitor load as compared with the diode–capacitor load.

6.2 Variant 2 - Double-Sided with Controlled Bias Voltage

To detect amplitudes of less than 0.57 V, a variant of the excessive swing detector has been developed (Figure 9). In the second type of built-in detector, an additional variable supply voltage (for test mode) is applied to the base of transistors Q4 and Q5 to increase the base-emitter bias voltage (VBE) of the detectors. With this change, the detector does not only check for excessive swings, but for all output signals going below the normal low level voltage.

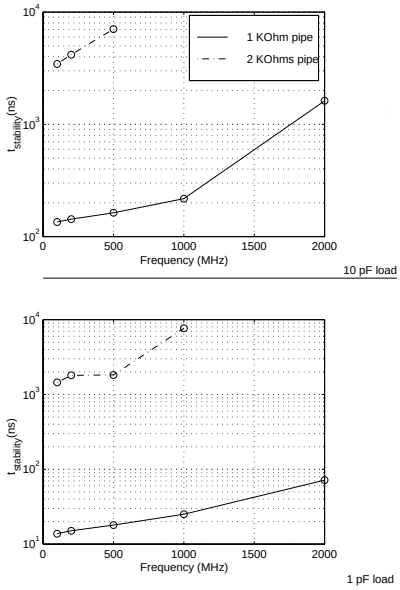


Figure 8 $\mathbf{t}_{stability}$ vs. frequency, pipe value and load capacitor (variant 1, diode)

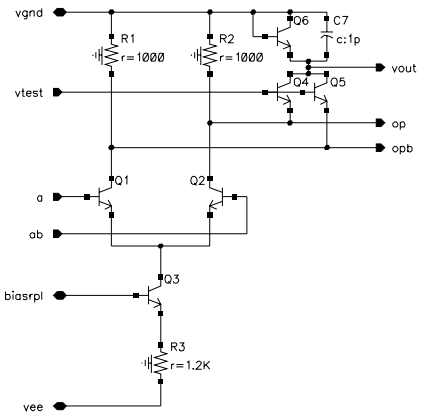


Figure 9 Proposed built-in detector (variant 2)

In variant 2, pin vtest is added and is set to vgnd in normal mode and set to a higher voltage in test mode. Raising vtest's voltage in test mode helps transistors Q4 and Q5 reach a sufficient forward bias when signals op or opb have an abnormally low transient voltage value, lower than the acceptable low level. If a fault leads to an abnormal swing at a gate output, transistors Q4 or Q5 will conduct enough to pull down the voltage on the diode-capacitor load. If the voltage values on *op* and *opb* remain in an acceptable interval, Q4 and Q5 will not conduct, leaving *vout* at *vgnd*.

Experiments similar to those conducted with variant 1 were performed with variant 2 of the detector. Depending on the transistors turn-on characteristics, it is beneficial to adjust *vtest*. A 3.7 V *vtest* value was found to be an excellent compromise for a V_{BE} = 900 mV technology. The results are reported in Figure 10.

These results show that the detectable amplitude value reduces down to about 0.35 V (equivalent to a 5 KΩ pipe on Q3), while $t_{stability}$ is much shorter than in variant 1.

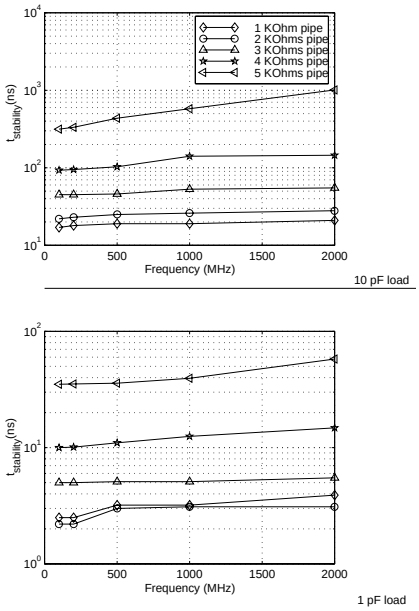


Figure 10 $\mathbf{t}_{stability}$ vs. frequency, pipe value and load capacitor (variant 2)

6.3 Conversion of Detector Output Voltage to a Logic Value

While the two diode-capacitor detectors presented in subsections 6.1 and 6.2 are quite efficient, their use unravels a common challenge: in the fault-free voltage range, they both exhibit a very high output impedance. This is challenging because bipolar comparators can have large input impedance, but this impedance is not as large as one may wish in the present case. Indeed, a CML buffer input always sinks some current from the incoming signal, whatever its logic value, and this current is somewhat larger when the input signal is a logic 1. For example, using variant 2 (Figure 9) if the cell being tested is fault-free, transistors Q4 and Q5 are open and *vout* should be kept at *vgnd* by the load circuit. But since a buffer input sinking current is not negligible, the load diode Q6 would be forced to supply that current, creating a voltage drop that lowers *vout*. In the circuits used, the buffer input current is large enough to pull down *vout* at a value comparable to that observed with a faulty circuit.

To overcome this challenge, a viable solution is proposed as seen in Figure 11. The load circuit supply connection was pulled up to vtest in order to let it supply the average input bias current required by the comparator, while keeping a high enough quiescent value on vout. Also, in order to increase the difference between vout in the faulty and fault-free cases, a resistor (R0) was added in parallel to the load circuit to reduce the drop caused by the comparator. Since the resistor has a smaller impedance than the diode in the small current region, the input bias current of the comparator flows mainly through the resistor, which reduces the voltage drop. The ideal load circuit parameters may need to be adjusted as a function of the cells speed/ power combination which is determined by the gate current source. Analysis shows that a 40 KΩ resistor value is a good choice when considering detection of amplitudes above 0.35 V.

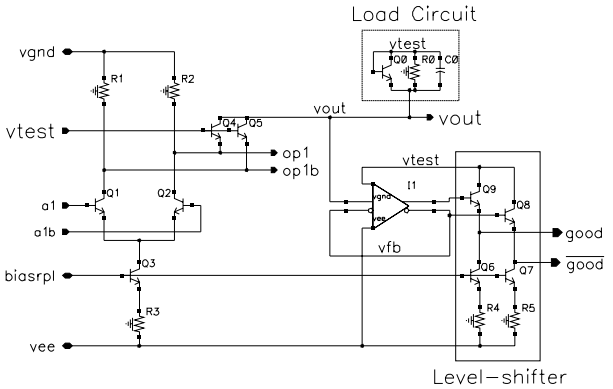


Figure 11 Amplitude detector (variant 3)

To decide if vout represents a good or a bad circuit, the comparator needs a voltage reference. Taking a fixed reference value centred between the expected vout value for a fault-free circuit and for a circuit with a 0.35 V amplitude is a good choice. However, even though the difference between those two values is close to a normal swing, as shown later on in Figure 14, the reference voltage value suggested would then yield a maximum of half a normal noise margin on the inputs of the comparator in the fault-free case. Thus, the standard noise margin would be recovered only after a few gates. The proposed solution is composed of two modifications, which are already shown in Figure 11. The first was to connect the comparator supply to *vtest*, in order for its outputs to be compatible for a comparison with *vout*. The second modification was to use a feedback on the comparator. Note that *vfb* in Figure 11 is not only the complementary output of the detection amplifier, but is also the feedback voltage (complementary input) to which *vout* is compared. This increases the noise margin and provides a sharper switching due to the positive feedback it introduces. Finally, to get back down to standard CML voltage levels, a level-shifter was used.

Excessive positive feedback could be harmful if it leads the comparator to deadlock in the defective state during some transitions, even though the device under test is good. Figure 12 characterizes the hysteresis due to the introduced positive feedback and confirms that a fault free gate will never be wrongly declared defective. With the current design, a defective gate yielding a vout of 3.54 V is guaranteed to be detected as a fault, whereas a

gate with a vout larger than 3.57 V would be treated as fault free.

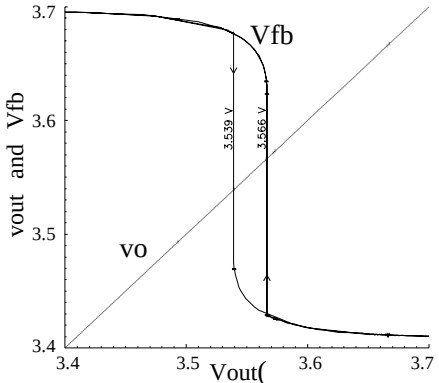


Figure 12 Hysteresis effect on the comparator

6.4 Load Sharing

In order to reduce the cost of the proposed method, part of the built-in detectors can be shared, namely the load circuit as well as the comparator as shown in Figure 13.

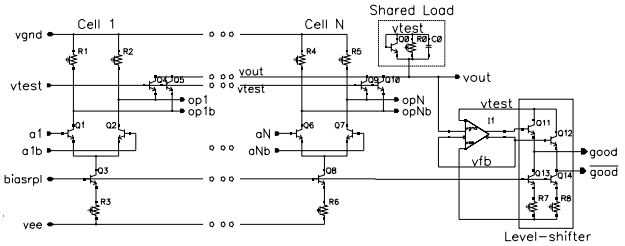


Figure 13 Load sharing for variant 3

To investigate the impact of sharing the load cell and the comparator over a number of detector outputs, the built-in detectors described above were simulated with a buffer chain of variable length (***N***). In the proposed configuration, each pair of outputs *op***i** and *op***i***b* of buffer **i** are connected to two dedicated detector transistors as shown in Figure 13.

In the first set of experiments, a number of detectors were connected together to a single shared load in a defect free circuit. The results for the fault-free circuit are reported in Figure 14.

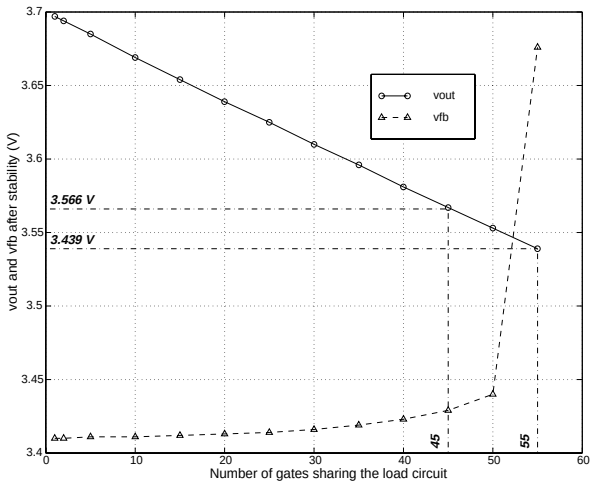


Figure 14 Detector response with a fault-free circuit

These results show that *vout* decreases linearly with the number of parallel cells as the leakage currents from the cells add up. This behaviour can be explained by the load circuit current-to-voltage relationship. Resistor R0 and transistor Q0 have both an effect on *vout*. In the load circuit, if the transistor was dominant, the effects on *vout* when increasing ***N*** would be logarithmic whereas a dominant resistor would yield a linear relationship between ***N*** and *vout*. In the present situation, R0 has a 40 KΩ value which is dominant over the transistor when it has low V_{BE} values. Therefore, in a fault-free circuit, where Q0's V_{BE} is small, R0 is dominant in the load circuit and yields a linear behaviour when load sharing increases. Changing the R0 value obviously changes the slope of the curve.

The results also show that, while the feedback keeps a noise margin higher than 50% on the comparator's input, a limit exists on the number of cells that can share the same load circuit. A good criterion to obtain a secure maximum number of buffers that can share the same load circuit, would require that *vout* exceeds the highest voltage of the hysteresis curve, which is 3.57 V. Figure 14 presented the low and high values of the hysteresis curve transposed from Figure 12, and according to the results, the safe maximum for sharing loads is 45 buffers.

For defective circuits exhibiting amplitudes greater than 0.35 V, simulations have shown that for ***N = 1***, the detector will give out a *vout* of 3.41 V. Knowing that sharing will only decrease *vout* (as shown in Figure 14), sharing will not obstruct fault detection when an amplitude fault is present.

Considering the small variations of the output voltage with the number of cells, and the more than sufficient residual noise-margin that allows to distinguish the faulty and fault-free circuits, it is clear that sharing a load cell and the associated comparator by up to 45 gates is feasible.

6.5 Area Optimization

An interesting refinement to the implementation of the detectors of variant 2 and 3 is to use multiple emitter transistors as shown in Figure 15. Instead of using two transistors (Q4 and Q5 of Figure 9) the detector can be implemented by one transistor with two emitters. This transistor configuration provides two inputs connected to the buffer's outputs *op* and *opb*. It allows a considerable reduction in the area overhead for circuits that use large numbers of detectors.

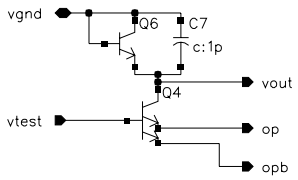


Figure 15 Area optimization by using multiple emitter transistors

6.6 Testing Approach

While pipe defects in current source transistors affect both output amplitudes and are fully detectable with DC test, in some more complex gates, some defects modify the amplitude of only one output and thus, masking the fault. To detect it, the fault must be asserted by sensitizing a path through the faulty gate and make its output toggle. In this case the fault is asserted half the cycles time. Since the detectors pull-down resistance on *vout* when the fault is asserted is much stronger than the load circuit pull-up resistance, capacitor C0 will stabilize *vout* at a low value and the amplitude detector will be able to flag the faulty gate.

For combinational circuits, getting a path to toggle is a question of applying test vectors to sensitize it, but for sequential circuits, it is not that simple. An effective method to obtain a good toggle coverage in a sequential circuit is to stimulate it with random patterns. Measuring the toggle coverage by simulation does pose the problem of finding an initialisation sequence. However, that objective is easily accomplished with most circuits, since as presented in [13], they tend to converge to a deterministic state, irrespective of the initial state, and that convergence is easily demonstrated with a single fault free simulation of relatively short length.

7. Conclusion

This paper has proposed a DFT technique to detect a class of parametric faults encountered in CML circuits. It consists in implementing built-in detectors at the output of each buffer gate. Instead of testing the circuits at the primary outputs, the testing is performed on all gate outputs through these built-in detectors. This method is very effective to detect degraded signals caused by classes of defects such as a collector to emitter pipe on the current source transistor. Three detector configurations have been proposed. Variant 1 allows to detect amplitude greater than 0.57 V, while the detectable excursion for variant 2 decreases down to 0.35 V. Variant 3 is an improvement that makes the detector more immune to noise. It was shown that a load cell can be shared by up to 45 gates and still detect an amplitude fault on one of them. A multiple emitter transistor configuration has also been proposed to reduce the number of transistors for variant 2 and 3. Finally, a testing scheme for output amplitude faults was proposed. It consists in sensitizing paths one after the other and applying toggling input signals. For sequential circuits, random patterns are suggested to yield good toggle coverage.

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