# Path Delay Fault Testing of ICs with Embedded Intellectual Property Blocks

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## Abstract

*In this paper we show that the already known method of using multiplexers for making the inputs and outputs of the embedded blocks accessible by the primary ports of the Integrated Circuit (IC) can be used for path delay fault testing of the IC. We show that the testing of the IC for path delay faults can be reduced to the testing of each block. Intellectual Property (IP) blocks are treated as black boxes. The number of the circuit paths that must be tested is almost equal to the sum of the paths that must be tested for each block.*

## 1. Introduction

The design effort and the time to market for an IC can be significantly reduced when pre-designed (either in-house or provided as third-party Intellectual Property -IP-) blocks are used. For this reason, the use of pre-designed blocks is being increasingly used for designing new complex ICs.

Like all other semiconductor devices, the chips being designed using pre-designed blocks must be well tested in production to become a viable product. Testing such pre-designed block based ICs is difficult due to the problem of justifying test sequences at the inputs of a block embedded deep in the IC and propagating test responses from the block outputs to the primary outputs of the IC. The problem is even more serious in the case of IP blocks, because they are considered as black boxes. Several techniques have been proposed to address this issue [1], test grid [2], boundary scan around each IP block [3], partial isolation rings [4], BIST techniques [5] and multiplexing to make the inputs and outputs of each IP block accessible at the primary ports of the IC [6]. The last may be difficult when there are more IP block inputs/outputs than chip pins or when routing is complex. However there are many cases that this method can be applied easily. For example, the circuit of Figure 1 is commonly found in Digital Signal Processors (DSPs). Consider that the shifter (multiplexer based) and the ALU are pre-designed by the same company and the multiplier is an IP block. Figure 2 presents the same circuit after the addition of the suitable multiplexers. We note that the 2:1 multiplexer at the outputs of the shifter and the multiplier in Figure 1 has been replaced by 3:1 multiplexer and a new 2:1 multiplexer has been added at the output of the ALU so that the inputs and the outputs of each block to be directly accessible by the data bus lines. The hardware overhead due to the multiplexer insertion is obviously negligible.

Increasing performance requirements of VLSI circuits makes it difficult to design them with large timing margins. Thus imprecise delay modelling, the statistical variations of the parameters during the manufacturing process as well as physical defects in the integrated circuits can sometimes degrade circuit performance without altering its logic functionality. These faults are called delay faults. There are two popular delay fault models. One is the gate delay fault model where delays violating specifications are assumed to be due to a single gate delay [7, 8]. The other is the path delay fault model where a path is declared faulty if it fails to propagate a transition from the path input to the path output within a specified time interval [9]. The latter model is deemed to be more general since it captures the cumulative effect of small delay variations in gates along a path as well as the faults caused by a single gate. A physical path of a circuit is an alternating sequence of gates and lines leading from a primary input to a primary output of the circuit. The number of physical paths in a contemporary circuit is prohibitively large in order for all the paths to be tested for path delay faults. To this end to reduce the paths that must be tested for path delay faults various path selection methods have been proposed (for example [10 - 13]) although none of them has been proven to be satisfactory for the general case.

In this paper we show that using the method of multiplexing, the path delay fault testing of an IC is

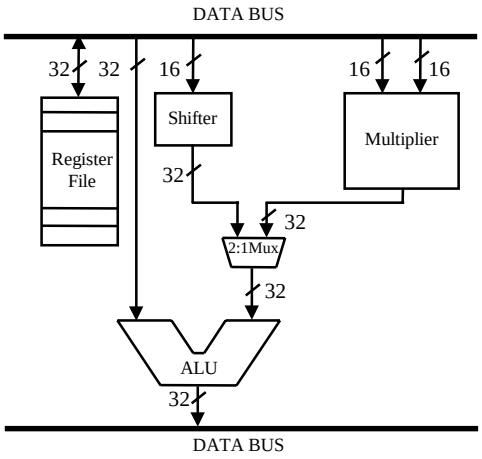


Figure 1. Common DSP Datapath.

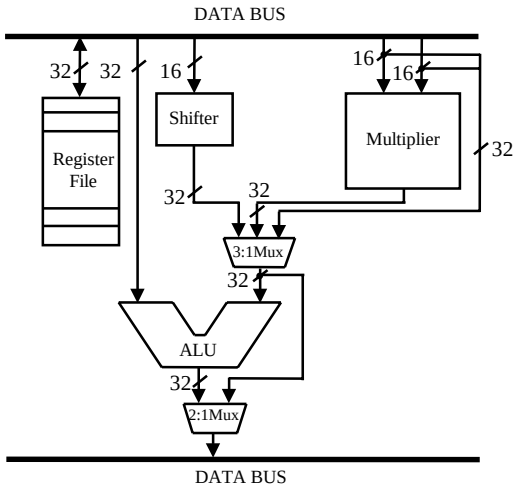


Figure 2. Modified DSP Datapath.

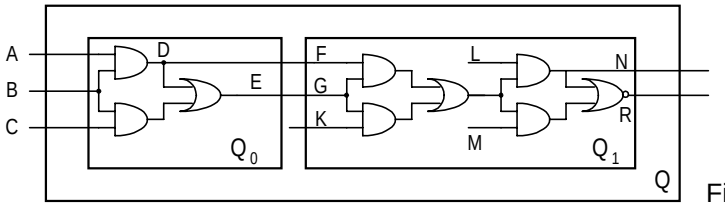


Figure 3.

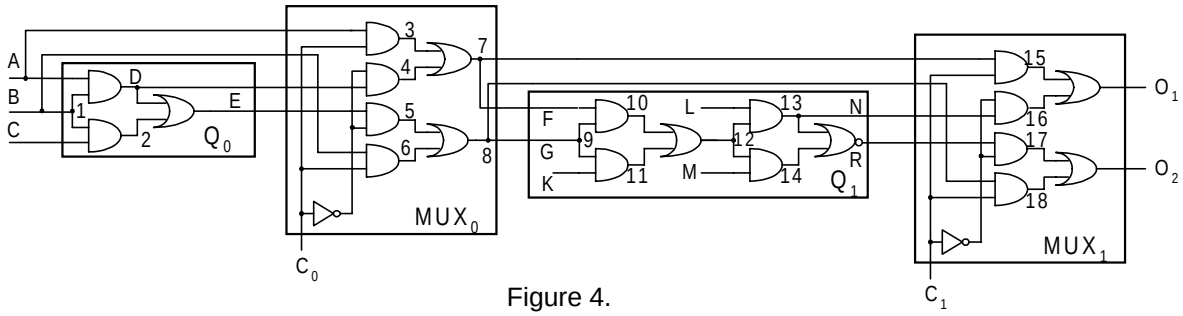


Figure 4.

reduced to the path delay fault testing of each of the blocks that constitute it. We also show that the cardinality of the test set of the IC is approximately equal to the sum of the cardinalities of the test sets of the blocks that constitute the IC. Considering that a compound circuit may have exponentially more physical paths than the sum of the physical paths of each subcircuit, this means that we achieve a significant reduction of the paths that must be tested. Another contribution of the paper is that the logical design of the blocks is not required. It is sufficient to only know the test set of each block for path delay faults, which is an information provided by the IP block vendor. Therefore, ICs with embedded IP Blocks can be tested for path delay faults.

## 2. Path Delay Fault Testing Method

The main idea behind our method is very simple. In the sequel we will exemplify the idea using a trivial circuit, that of Figure 3. If we consider the blocks $Q_0$ and $Q_1$ as stand-alone, then they have 6 and 15 physical paths respectively, that are all robustly testable [14]. Considering on the other hand blocks $Q_0$ and $Q_1$ as one circuit Q, the number of physical paths is equal to 36, that is significantly more than the sum of the physical paths of the blocks $Q_0$ and $Q_1$.

Inserting multiplexers in the circuit of Figure 3 and connecting the embedded inputs and outputs of each subcircuit to those primary inputs and outputs that are not used by the subcircuit under test we get the circuit of Figure 4. In realistic circuits the pre-designed blocks, $Q_0$ and $Q_1$ in this example, have thousand of gates, so the hardware overhead due to multiplexer insertion is negligible. For $C_0 = C_1 = 0$ the outputs of $Q_0$ drive the inputs F and G of $Q_1$. For $C_0 = 0$ and $C_1 = 1$ the outputs of $Q_0$ drive the primary outputs $O_1$ and $O_2$ of the circuit. For $C_0 = 1$ and $C_1 = 0$ the inputs F and G of $Q_1$ are driven from

the primary inputs A and B of the circuit, while its outputs N and R drive the primary outputs $O_1$ and $O_2$ of the circuit. The physical paths of the circuit of Figure 4 for $C_0 = C_1 = 0$ are given in Table I. We have to note that the multiplexers $MUX_0$ and $MUX_1$ do not increase the number of paths, that is, if the outputs of $Q_0$ were connected directly to the inputs of $Q_1$ and all outputs of $Q_1$ were primary outputs, the total number of paths would be the same.

Assuming that all paths of the circuit of Figure 4 must be tested for path delay faults (a path selection method is not used) we conclude that the propagation delay along any one path of Table I must be measured. Tables II and III respectively list the physical paths that go only through $Q_0$ ($C_0 = 0$, $C_1 = 1$) or $Q_1$ ($C_0 = 1$, $C_1 = 0$). The testing of the circuit of Figure 4 for path delay faults, that is, the measurement of the propagation delays along the physical paths of Table I is reduced to the measurement of the propagation delays along the paths of Tables II (path delay fault testing of $Q_0$) and III (path delay fault testing of $Q_1$) and the following two paths :

P' = A-3-7-15-$O_1$

P" = B-6-8-18-$O_2$.

The propagation delay along each physical path of Table I can be calculated as a function of the propagation delays along a path of Table II, a path of Table III and one of the paths P' or P". For example the propagation delay of a 0->1 or 1->0 transition along the paths $P_9$ and $P_{19}$ can be calculated as :

$d(P_9) = d(P_{0,2}) + d(P_{1,0}) - d(P')$ and

$d(P_{19}) = d(P_{0,4}) + d(P_{1,4}) - d(P")$.

The propagation delay along any other physical path of Table I can be calculated in the same way. The propagation delay along the paths with inputs $C_0$ and $C_1$ have not been considered because during normal operation of the circuit $C_0 = C_1 = 0$. During test mode the inputs $C_0$ and $C_1$ change values only three times so we can wait enough time before applying the test sets.

In this trivial circuit of Figure 4 the number of physical paths along which the propagation delay must be measured is equal to 6 + 15 + 2 = 23 while the number of all physical paths is 36. In realistic circuits consisting of two or more blocks the physical paths of the circuit may be several

Table I. Physical Paths of the circuit of Figure 4 for $C_0 = C_1 = 0$.

| | |
|---|---|
| $P_0$ | A-D-4-7-F-10-12-13-N-16-$O_1$ |
| $P_1$ | A-D-4-7-F-10-12-13-R-17-$O_2$ |
| $P_2$ | A-D-4-7-F-10-12-14-R-17-$O_2$ |
| $P_3$ | A-D-E-5-8-G-9-10-12-13-N-16-$O_1$ |
| $P_4$ | A-D-E-5-8-G-9-10-12-13-R-17-$O_2$ |
| $P_5$ | A-D-E-5-8-G-9-10-12-14-R-17-$O_2$ |
| $P_6$ | A-D-E-5-8-G-9-11-12-13-N-16-$O_1$ |
| $P_7$ | A-D-E-5-8-G-9-11-12-13-R-17-$O_2$ |
| $P_8$ | A-D-E-5-8-G-9-11-12-14-R-17-$O_2$ |
| $P_9$ | B-1-D-4-7-F-10-12-13-N-16-$O_1$ |
| $P_{10}$ | B-1-D-4-7-F-10-12-13-R-17-$O_2$ |
| $P_{11}$ | B-1-D-4-7-F-10-12-14-R-17-$O_2$ |
| $P_{12}$ | B-1-D-E-5-8-G-9-10-12-13-N-16-$O_1$ |
| $P_{13}$ | B-1-D-E-5-8-G-9-10-12-13-R-17-$O_2$ |
| $P_{14}$ | B-1-D-E-5-8-G-9-10-12-14-R-17-$O_2$ |
| $P_{15}$ | B-1-D-E-5-8-G-9-11-12-13-N-16-$O_1$ |
| $P_{16}$ | B-1-D-E-5-8-G-9-11-12-13-R-17-$O_2$ |
| $P_{17}$ | B-1-D-E-5-8-G-9-11-12-14-R-17-$O_2$ |
| $P_{18}$ | B-1-2-E-5-8-G-9-10-12-13-N-16-$O_1$ |
| $P_{19}$ | B-1-2-E-5-8-G-9-10-12-13-R-17-$O_2$ |
| $P_{20}$ | B-1-2-E-5-8-G-9-10-12-14-R-17-$O_2$ |
| $P_{21}$ | B-1-2-E-5-8-G-9-11-12-13-N-16-$O_1$ |
| $P_{22}$ | B-1-2-E-5-8-G-9-11-12-13-R-17-$O_2$ |
| $P_{23}$ | B-1-2-E-5-8-G-9-11-12-14-R-17-$O_2$ |
| $P_{24}$ | C-2-E-5-8-G-9-10-12-13-N-16-$O_1$ |
| $P_{25}$ | C-2-E-5-8-G-9-10-12-13-R-17-$O_2$ |
| $P_{26}$ | C-2-E-5-8-G-9-10-12-14-R-17-$O_2$ |
| $P_{27}$ | C-2-E-5-8-G-9-11-12-13-N-16-$O_1$ |
| $P_{28}$ | C-2-E-5-8-G-9-11-12-13-R-17-$O_2$ |
| $P_{29}$ | C-2-E-5-8-G-9-11-12-14-R-17-$O_2$ |
| $P_{30}$ | K-11-12-13-N-16-$O_1$ |
| $P_{31}$ | K-11-12-13-R-17-$O_2$ |
| $P_{32}$ | K-11-12-14-R-17-$O_2$ |
| $P_{33}$ | L-13-N-16-$O_1$ |
| $P_{34}$ | L-13-R-17-$O_2$ |
| $P_{35}$ | M-14-R-17-$O_2$ |

Table II. Physical paths that go through $Q_0$ for $C_0$=0 and $C_1$=1

| | |
|---|---|
| $P_{0,0}$ | A-D-4-7-15-$O_1$ |
| $P_{0,1}$ | A-D-E-5-8-18-$O_2$ |
| $P_{0,2}$ | B-1-D-4-7-15-$O_1$ |
| $P_{0,3}$ | B-1-D-E-5-8-18-$O_2$ |
| $P_{0,4}$ | B-1-2-E-5-8-18-$O_2$ |
| $P_{0,5}$ | C-2-E-5-8-18-$O_2$ |

Table III. Physical paths that go through $Q_1$ for $C_0$=1 and $C_1$=0

| | |
|---|---|
| $P_{1,0}$ | A-3-7-F-10-12-13-N -16-$O_1$ |
| $P_{1,1}$ | A-3-7-F-10-12-13-R-17-$O_2$ |
| $P_{1,2}$ | A-3-7-F-10-12-14-R-17-$O_2$ |
| $P_{1,3}$ | B-6-8-G-9-10-12-13-N-16-$O_1$ |
| $P_{1,4}$ | B-6-8-G-9-10-12-13-R-17-$O_2$ |
| $P_{1,5}$ | B-6-8-G-9-10-12-14-R-17-$O_2$ |
| $P_{1,6}$ | B-6-8-G-9-11-12-13-N-16-$O_1$ |
| $P_{1,7}$ | B-6-8-G-9-11-12-13-R-17-$O_2$ |
| $P_{1,8}$ | B-6-8-G-9-11-12-14-R-17-$O_2$ |
| $P_{1,9}$ | K-11-12-13-N-16-$O_1$ |
| $P_{1,10}$ | K-11-12-13-R-17-$O_2$ |
| $P_{1,11}$ | K-11-12-14-R-17-$O_2$ |
| $P_{1,12}$ | L-13-N-16-$O_1$ |
| $P_{1,13}$ | L-13-R-17-$O_2$ |
| $P_{1,14}$ | M-14-R-17-$O_2$ |

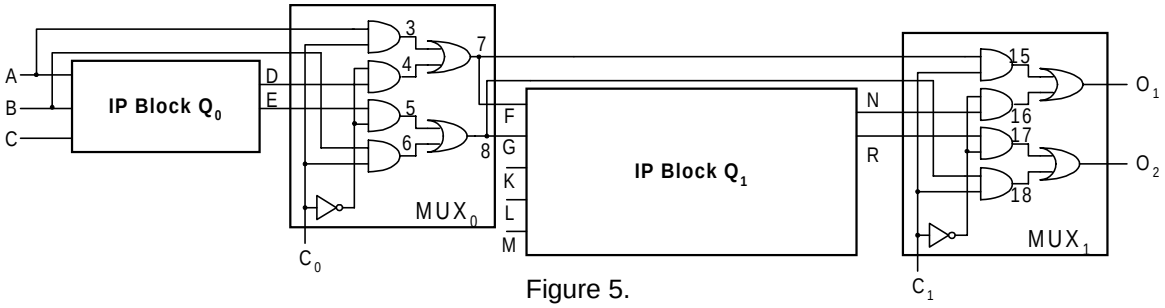


Figure 5.

orders of magnitude larger than the sum of the physical paths of each block. Furthermore, a circuit Q consisting of blocks that stand-alone are robustly testable, may not be robustly testable [14]. Ignoring the problem that stems from the possible extremely large number of physical paths of Q, the fact that is not robustly testable increases the difficulty of testing it for path delay faults. Following our method each block is tested as a robustly testable block and the delays along the physical paths of Q are calculated. From the above we conclude that our method reduces impressively the path delay fault testing effort.

## 3. Application to ICs with embedded IP blocks

In the sequel we will consider that blocks $Q_0$ and $Q_1$ are IP blocks (Figure 5). Therefore the vendors of $Q_0$ and $Q_1$ have provided us with their test sets for path delay fault testing but not with their designs. We do not know if the vendors, based on a path selection method, have considered that the propagation delay along a subset of all the physical paths or all the physical paths of the circuit must be measured. Assume that the vendors have provided us with the test sets in the form presented in Tables IV and V. Consider the first row of Table IV where A=T, B=1, C=0 and D=E=T. This is a compact way to denote that three test vectors ABC = 010, 110 and 010 must be applied to $Q_0$ and the correct responses are DE = 00, 11 and 00. Consider a row of Table IV or V. For each pair of an input I and an output O with value T we define a virtual path VP(I, O). For example the first row of Table IV defines two virtual paths, $VP_{0,1}$(A, D) and $VP_{0,2}$(A, E) while the third line defines only one $VP_{0,5}$(B,E). The virtual paths for an IP block represent what the physical paths represent in a block with known logic design. Path delay fault testing of $Q_0$ and $Q_1$ requires the measurement of the propagation delay along the 6 and 15 virtual paths respectively given in Tables IV and V.

Multiplexer $MUX_0$ connects a specific output $Y_i$ of $Q_0$ to specific input $Z_i$ of $Q_1$ where $i \in [1, n]$ and n is the number of outputs of $Q_0$ that drive inputs of $Q_1$. Path delay fault testing of the circuit of Figure 5 requires the measurement of the propagation delay along all the paths which include a virtual path of $Q_0$ with output $Y_i$, the sub-path $Y_i$-$Z_i$ of $MUX_0$ and a virtual path of $Q_1$ with input $Z_i$. Obviously if there exist $VP_{Yi}$ virtual paths of $Q_0$ with output $Y_i$ and $VP_{Zi}$ virtual paths of $Q_1$ with inputs $Z_i$, then there exists $VP_{Yi} * VP_{Zi}$ paths that the propagation along them must be measured. Assuming that $Q_0$ has n outputs that drive inputs of $Q_1$ the set of the paths become $\sum_{i=1}^{n} (VP_{Yi} * VP_{Zi})$. Let VP' be the set of virtual paths of $Q_0$ with outputs primary outputs of the circuit and VP" the set of virtual paths of $Q_1$ with inputs primary inputs of the circuit. Then the set of all paths along which the propagation delay must be measured is equal to :

$$VP' + VP'' + \sum_{i=1}^{n} (VP_{Yi} * VP_{Zi}).$$

Table IV. The test set and the responses for path delay faults of $Q_0$ given by the vendor

| Test vectors | Responses | Virtual Paths |
|---|---|---|
| ABC | DE | $VP_0$ |
| T10 | TT* | $VP_{0,1}$(A,D), $VP_{0,2}$(A,E) |
| 1T0 | TT | $VP_{0,3}$(B,D), $VP_{0,4}$(B,E) |
| 0T1 | X[t]T | $VP_{0,5}$(B,E) |
| 01T | XT | $VP_{0,6}$(C,E) |

* T denotes a transition 0->1 or 1->0

[t] X denotes that the vendor of $Q_0$ does not provide us with that value

Table V. The test set and the responses for path delay faults of $Q_1$ given by the vendor

| Test vectors | Responses | Virtual Paths |
|---|---|---|
| FGKLM | NR | $VP_0$ |
| T1001 | XT'* | $VP_{1,1}$(F,R) |
| T1010 | TT' | $VP_{1,2}$(F,N),$VP_{1,3}$(F,R) |
| 1T001 | XT' | $VP_{1,4}$(G,R) |
| 1T010 | TT' | $VP_{1,5}$(G,N),$VP_{1,6}$(G,R) |
| 0T101 | XT' | $VP_{1,7}$(G,R) |
| 0T110 | TT' | $VP_{1,8}$(G,N),$VP_{1,9}$(G,R) |
| 110T0 | TT' | $VP_{1,10}$(L,N),$VP_{1,11}$(L,R) |
| 1100T | XT' | $VP_{1,12}$(M,R) |
| 01T01 | XT' | $VP_{1,13}$(K,R) |
| 01T10 | TT' | $VP_{1,14}$(K,N),$VP_{1,15}$(K,R) |

* T' denotes the opposite to T transition.

According to the above, we must know the propagation delays along the following paths :

a. $VP_{0,i}$(I,D)-4-7-F-$VP_{1,2}$(F,N)-16-$O_1$ where I∈ {A,B} and i∈ {1, 3} (follows from Table IV).
b. $VP_{0,i}$(I,D)-4-7-F-$VP_{1,m}$(F,R)-17-$O_2$ where I∈ {A,B} i∈ {1, 3} and m∈ {1, 3}.
c. $VP_{0,j}$(I,E)-5-8-G-$VP_{1,s}$(G,N)-16-$O_1$ where I∈ {A,B,C}, j∈ {2, 4, 5, 6} and s∈ {5, 8}.
d. $VP_{0,j}$(I,E)-5-8-G-$VP_{1,t}$(G,R)-17-$O_2$ where I∈ {A,B,C}, j∈ {2, 4, 5,6} and t∈ {4, 6, 7, 9}.
e. $VP_{1,10}$(L,N)-16-$O_1$.
f. $VP_{1,11}$(L,R)-17-$O_2$.
g. $VP_{1,12}$(M,R)-17-$O_2$.
h. $VP_{1,14}$(K,N)-16-$O_1$.
k. $VP_{1,r}$(K,R)-17-$O_2$ with r∈ {13, 15}.

We note that a, b, c, d and k above represent groups of paths.

The propagation delays along the following paths can easily be measured :

i. $VP_{0,i}$(I,D)-4-7-15-$O_1$ with I∈ {A,B} and for i =1, 3.
ii. $VP_{0,j}$(I,E)-5-8-18-$O_2$ with I∈ {A,B,C} and for j=2,4,5,6.
iii. A-3-7-F-$VP_{1,2}$(F,N)-16-$O_1$.
iv. A-3-7-F-$VP_{1,m}$(F,R)-17-$O_2$ for m = 1, 3.
v. B-6-8-G-$VP_{1,s}$(G,N)-16-$O_1$ for s=5, 8.
vi. B-6-8-G-$VP_{1,t}$(G,R)-17-$O_2$ for t = 4, 6, 7, 9.
vii. A-3-7-15-$O_1$.
viii. B-6-8-18-$O_2$

and the paths e, f, g, h and k.

The paths vii and viii go only through $MUX_0$ and $MUX_1$.

We can easily see that the propagation delays along the paths of each of the groups a, b, c and d can be calculated respectively as a function of the propagation delays along the paths of groups (i, iii, vii), (i, iv, vii), (ii, v, viii) and (ii, vi, viii) as follows :

$d(VP_{0,i}(I,D)\text{-}4\text{-}7\text{-}F\text{-}VP_{1,2}(F,N)\text{-}16\text{-}O_1) = d(VP_{0,i}(I,D)\text{-}4\text{-}7\text{-}15\text{-}O_1) + d(A\text{-}3\text{-}7\text{-}F\text{-}VP_{1,2}(F,N)\text{-}16\text{-}O_1) - d(A\text{-}3\text{-}7\text{-}15\text{-}O_1)$, with I ∈ {A, B} and for i =1, 3,

$d(VP_{0,i}(I,D)\text{-}4\text{-}7\text{-}F\text{-}VP_{1,m}(F,R)\text{-}17\text{-}O_2) = d(VP_{0,i}(I,D)\text{-}4\text{-}7\text{-}15\text{-}O_1) + d(A\text{-}3\text{-}7\text{-}F\text{-}VP_{1,m}(F,R)\text{-}17\text{-}O_2) - d(A\text{-}3\text{-}7\text{-}15\text{-}O_1)$ with I ∈ {A, B} and m ∈ {1, 3},

$d(VP_{0,j}(I,E)\text{-}5\text{-}8\text{-}G\text{-}VP_{1,s}(G,N)\text{-}16\text{-}O_1) = d(VP_{0,j}(I,E)\text{-}5\text{-}8\text{-}18\text{-}O_2) + d(B\text{-}6\text{-}8\text{-}G\text{-}VP_{1,s}(G,N)\text{-}16\text{-}O_1) - d(B\text{-}6\text{-}8\text{-}18\text{-}O_2)$ with I ∈ {A, B, C}, j ∈ {2, 4, 5, 6} and s ∈ {5, 8} and

$d(VP_{0,j}(I,E)\text{-}5\text{-}8\text{-}G\text{-}VP_{1,t}(G,R)\text{-}17\text{-}O_2) = d(VP_{0,j}(I,E)\text{-}5\text{-}8\text{-}18\text{-}O_2) + d(B\text{-}6\text{-}8\text{-}G\text{-}VP_{1,t}(G,R)\text{-}17\text{-}O_2) - d(B\text{-}6\text{-}8\text{-}18\text{-}O_2)$ with I ∈ {A, B, C}, j ∈ {2, 4, 5, 6} and t ∈ {4, 6, 7, 9}.

Therefore, the propagation delays along the paths of the circuit of Figure 5 are calculated as a function of the propagation delays along the paths of the IP blocks $Q_0$ and $Q_1$. It is evident that the measurement of the propagation delays along $VP' + VP'' + \sum_{i=1}^{n} (VP_{Yi} * VP_{Zi})$ paths is reduced to the measurement of the propagation delays along $VP' + VP'' + \sum_{i=1}^{n} VP_{Yi} + \sum_{i=1}^{n} VP_{Zi}$ + n paths, where the last term denotes the number of paths only going through $MUX_0$ and $MUX_1$.

## 4. Conclusions

We have shown that, using multiplexers for making the inputs and outputs of the embedded blocks accessible by the primary ports of the IC, the path delay fault testing of the IC is reduced to the path delay fault testing of the blocks that constitute it. The above cuts down the test effort as well as the test application time significantly. Furthermore, ICs with embedded IP blocks can be tested for path delay faults.

## References


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