PANEL: WHAT IS THE PROPER SYSTEM ON CHIP DESIGN METHODOLOGY?

Chair: Richard Goering, EE Times, Felton, CA
Organizer: Stanley J. Krolikoski, Cadence Design Systems, San Jose, CA

Over the past year two distinct answers have emerged regarding SoC design methodologies. On the one hand, it is posited in the Reuse Methodology Manual, that a logic synthesis-based design methodology can be used effectively to develop system chips. An alternative methodology focuses on integration (or "reference") platforms and the customization of the basic application-specific platform through the addition of selected SW and/or HW IP blocks. This panel session will debate the merits of these seemingly incompatible proposed SoC methodologies.

Pierre Bricaud, Mentor Graphics, Sophia Antipolis, France

Obviously there is no one proper SoC design methodology. You don't design 3G GSM systems as you would Set Top Boxes or Graphics SoCs . But there is a proper design methodology and process to ensure that the components you will use for your SoC integration and verification meet your time to market and cost objectives. The key to this process is to use Reusable IPs and do a proper test and verification plan during SoC specifications . This implies that whatever form of the IP, Soft-Firm-Hard, it must be reusable to a known and accepted methodology, for example RMM and a well defined system verification software and hardware environment. Our contention that today the only complete pratical next generation digital SoC verification environment is based on hardware emulation that accomodates all representations of the IP, synthesizable testbenches and non-synthesizable testbenches, in-circuit emulation, software debugging, various memory configurations . The higher level of abstraction model or flexible PCB solutions cannot offer a valid solution for the next millinium SoCs .

James G. Dougherty, Integrated Systems Silicon LTD, Belfast, Northern Ireland

ISS and its design technology/methodology has been established in the knowledge that SoC design requires an entirely new mindset, which leaves behind the old attitudes and habits of the ASIC and full custom IC era.

If it is believed that SoC is inevitable, there have to be much improved levels of design productivity, many times higher than is possible with today's approaches to EDA, and every design team will have to use them. Design reuse is much vaunted, but current levels of understanding of the engineering challenges are basic, and consequently there are no EDA tools for building complex and deeply reuseable IP. Much innovation is required.

The industry is discovering painfully slowly that entirely new design methodologies are required to provide the industry with the productivity demanded by market timescales. The availability of truly reuseable, reconfigurable, functional IP blocks that are quickly built and verified, are plug 'n' play, are process non-specific and are guaranteed to work first time, must be prime goal of the SoC industry

Steve Glaser, Cadence Design Systems, San Jose, CA, USA

Design reuse has, so far, been approached from a very IC centric view, rather than a system centric view. The IC centric view tends to be 'authoring driven'…focused on the creation of blocks that can be stored in a big library, adhering to certain style guides and format standards so that someone else can use the source code, modify it, re-implement it, and re-verify it. This of course takes a tremendous amount of time…especially as the block get larger, more complicated, more application specific, and deep sub-micron issues make them more unpredictable. Unfortunately, designers get anywhere from .5x (takes twice as long as doing it themselves from scratch) to 2x productivity for a given IP integration task.

Therefore, as one proceeds to system on a chip, the more system-centric view must take over. This tends to be very 'integration driven'. So just as physical component providers target specific system performance and interface specs, virtual component/block designers must do the same if integration productivity is going to be increased.

Michael Keating, Synopsys Inc, Mountain View, CA, USA

The most critical success factor for SoC design now, and in the future, is the quality of the blocks, the IP, that are integrated into the chip design. Nothing you do in the integration flow can make up for poorly designed IP. Well-designed IP can be integrated into a wide variety of flows.

To produce these high quality pieces of IP, it is essential to adopt a disciplined design style that restricts the design space to scalable, portable, easy-to-integrate designs. This means fully synchronous designs, registered inputs and outputs, rigorous verification, and good specifications.

In my current thinking, the distinctions between hard and soft IP are blurring. I see all IP as starting out soft; many will have hard views. But the GDSII is just another view of the IP. The fundamental distinction between IP is in quality. Well-designed IP, whether in its hard or soft view, is the key to successful SoC design.

Robert Payne, VLSI Technology, San Jose, CA, USA

I shall describe the extent to which highly tuned "silicon craftsmanship" is required to implement the high performance mixed signal and special physical interfaces needed to be effective with SoC. The productivity and risk dilemmas, faced by system development teams, will be defined. A focus on new SoC methodology rather than tools is expected to provide the solution. I shall introduce a new development paradigm called the "Rapid Silicon Prototyping" design style, and will show how it leverages "Parameterized Intellectual Property" design reuse. I shall also

describe how it addresses the productivity and risk dilemmas. The need for efficient IP migration to the latest process generation will be shown to be essential to take full advantage of deep submicron technology. The VLSI Velocity(TM) product family will provide a real life example of how Rapid Silicon Prototyping is being deployed in industry.

Davoud Samani, Siemens Semiconductor, Munich, Germany

The National Technology Roadmap for Semiconductors predicts that, by the year 2005, the leading-edge designs will exceed 200M transistors operating at across-the-chip frequency of 1GHZ. With the current productivity, 100-gates/designer day, no serious company could stand the associated cost and design cycle. Deep sub-micron process technologies are creating, through their capability to integrate a complete system on a chip, a profound paradigm shift in system/IC design, test and fabrication. Without any doubt, reusable IP constitutes the cornerstone of new design paradigm, admitting to achieve low cost, short design cycle and high quality in multi-million-gate ICs.

Our everyday concerns (challenges?) to shift to this new design paradigm are the following:

- How to incentive design-for-reuse culture in company
- How to create efficiently all necessary views for various macros
- How to integrate digital, analog and mixed-signal blocks into a SOC design
- How to verify functionality and timing in complex systems
- How to warrant quality of design in terms of area, performance, power consumption
- How to ensure signal integrity and signal reliability
- How to carry out failure analysis on multi-layer-metal complex embedded ICs

Failure to quantify and address these issues will compromise the substantial investment being made in the process technology development and consequently the future of electronic industry.