Interconnect Analysis: From 3-D Structures to Circuit Models

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Abstract

In this survey paper we describe the combination of: discretized integral formulations, sparsification techniques, and krylov-subspace based model-order reduction that has led to robust tools for automatic generation of macromodels that represent the distributed RLC effects in 3-D interconnect. A few computational results are presented, mostly to point out the problems yet to be addressed.

1 Introduction

Until very recently, processor designers who worried about interconnect inductance have been dismissed as alarmists. There were a small number of clock distribution experts who were well aware of inductive effects, but these experts failed to change the prevailing view because of their small population and the proprietary nature of their work. The recent use of on-chip ground planes to minimize inductance has made it clear that inductive effects have a serious impact on processor design [1].

Developers of computer-aided design tools which handle inductive effects were undetered by the lack of designer enthusiam for such capabilities. Instead, tools were developed for modeling the distributed RLC effects in interconnect. These tools begin with 3-D structures generated from a layout description, and produce low-order systems of equations suitable for use in a circuit-level simulation.

In this survey paper we describe, in limited technical detail, the combination of algorithms that makes possible the automatic generation of circuit models from 3-D distributed RLC analysis. In the next section we describe the system of equations generated by the commonly used discretized integral formulations for the RLC problem, and then in section three we present some of the ideas behind the fast algorithms used to solve these equations. In section four we describe a little about the Krylov-subspace based model order reduction techniques. In section five we present some of the problems that these recent developments have uncovered.

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2 Discretized Integral Formulation

On-chip interconnect can be treated quasistatically, in which case the integral formulation of the Laplace transformed Maxwell's equations can be represented as

$$s\frac{\mu}{4\pi}\int_D \frac{\boldsymbol{J}(\boldsymbol{r}',s)}{|\boldsymbol{r}-\boldsymbol{r}'|}dv' + \frac{\boldsymbol{J}(\boldsymbol{r},s)}{\sigma} = -\nabla\Phi(\boldsymbol{r},s), \quad (1)$$

where s is the Laplace frequency, D is the interior of all conductors, r is a position in the interior. The interior current density, $\boldsymbol{J}$, satisfies

$$\nabla\cdot\boldsymbol{J}(\boldsymbol{r},s) = 0 \quad (2)$$

and the scalar potential Φ satisfies

$$s\Phi(\boldsymbol{r},s) = \frac{1}{4\pi\epsilon}\int_S \frac{\boldsymbol{n}\cdot\boldsymbol{J_s}(\boldsymbol{r}',s)}{|\boldsymbol{r}-\boldsymbol{r}'|}dv', \quad (3)$$

where S is the surface of all conductors and $\boldsymbol{n}\cdot\boldsymbol{J_s}(\boldsymbol{r}',s)$ is the normal current density on the surface.

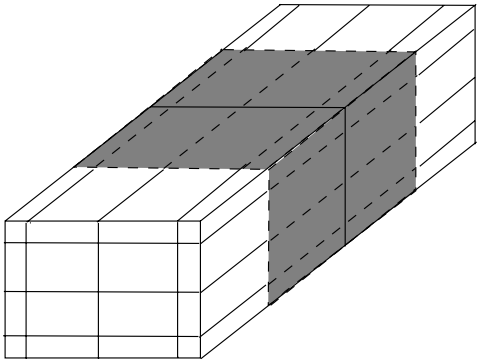

Figure 1: Discretization of a short conductor. The volume is discretized into current carrying parallel filaments along the length and the surface is discretized into panels shaded in gray.

At sufficently high frequencies, or for sufficiently thin conductors, (1), (2) and (3) can be simplified to involve only currents and potentials on the conductor surfaces. Such analyses are often referred to as "$2\frac{1}{2}$-D" analyses in layered media, or skin-depth approximations for general 3-D geometries. Since the skin depth of aluminum is of the order of microns at one gigahertz, such approximations should be checked.

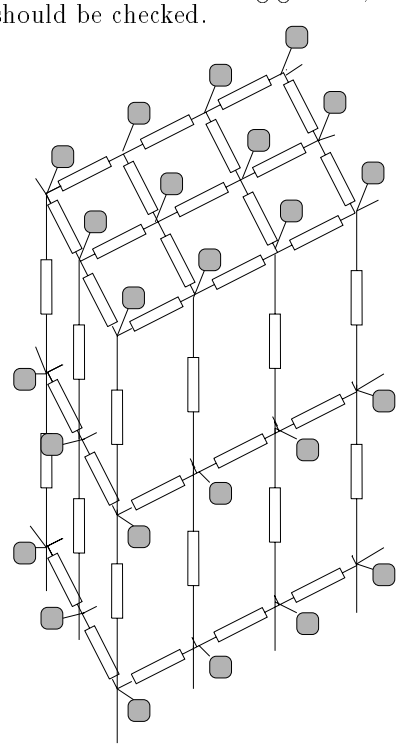

Figure 2: Discretization of conductor into current carrying filaments and charge carrying panels. Rectangles are filaments, shaded squares are panels.

In order to generate a well-conditioned discretized system, it has often been observed that the curl-free and divergence-free parts of the current should be represented seperately [2, 3, 4]. As a simple way of seeing how this is accomplished is to consider using a PEEC discretization [5], in which conductor volumes are sliced into thin filaments and conductor surfaces are broken into panels (see Figure 1). When viewed as interconnected current-carrying elements, as in Figure 2, it is possible to introduce mesh currents which either pass through loops of filaments; or enter through one panel, pass through a single filament, and leave through a second panel. Since the mesh currents always enter and then leave a node, they represent divergence free current. Let M^T be the matrix which, when multiplied by the mesh currents, yields the filament currents. Also, let A_p denote the panel incidence matrix. Then,

$$\begin{aligned} s \begin{bmatrix} L_m & 0 \\ 0 & I \end{bmatrix} \begin{bmatrix} I_m \\ V_p \end{bmatrix} = \\ \begin{bmatrix} -R_m & -MA_p \\ P\,(MA_p)^T & 0 \end{bmatrix} \begin{bmatrix} I_m \\ V_p \end{bmatrix} + \begin{bmatrix} V_s \\ 0 \end{bmatrix} \\ s\mathcal{L}\,\boldsymbol{x} = -\mathcal{R}\,\boldsymbol{x} \;+\; \boldsymbol{B}\,V_t \\ I_t = \boldsymbol{B}^T \boldsymbol{x}. \end{aligned} \tag{4}$$

where $L_m = MLM^T$ is the dense mesh inductance matrix, $R_m = MRM^T$ is the sparse mesh resistance matrix, P is the electrostatic potential coefficient matrix, and $\mathcal{R}$ and $\mathcal{L}$ are defined as the block matrices of (4) [6].

3 Sparsification Techniques

If direct factorization is used to solve (4) for the admittance at a given frequency, then since L_m and P are dense, the memory required to store the matrix will grow like n^2 and the matrix solve time will increase like n^3. If instead, a preconditioned Krylov-subspace method is used to solve for the admittance, then it is possible to reduce the solve time to order n^2 but the memory requirement will not decrease.

In order to develop algorithms which reduce memory and cpu time use, it is essential *not* to form the matrix explicitly. Instead, one can exploit the fact that Krylov-subspace methods for solving systems of equations only require matrix-vector products and not an explicit representation of the matrix. For example, note that for P in (4), computing Pq is equivalent to computing n potentials due to n sources. The potentials can be computed approximately in nearly order n operations by using an implicitly defined sparse representation of P [7, 8, 9]. Several researchers simultaneously observed the power of combining discretized integral formulations, Krylov-subspace methods, and implicit sparsification [10, 11].

Early general 3-D codes using sparsification were applied to capacitance extraction, and were based on the fast multipole algorithm [12, 13]. The approach has been used to compute inductance [14], and the basic algorithms have been improved by incorporating better adaptivity, higher-order elements and improved efficiency for high accuracy [15, 16, 17]. In addition, much recent work has focussed on allowing for more general Greens functions like those associated with layered media. There is the panel clustering idea [11], a multigrid style method [18], projection to a uniform grid combined with the FFT [9, 19] a technique based on the singular-value decomposition [4], and approaches based on using wavelet-like methods [20, 21, 22].

4 Model-Order reduction

The now-standard approach to efficient circuit-interconnect simulation is to represent the interconnect with moment-matching based reduced order models [23, 24, 25, 26]. Accurate computation of such models can be accomplished using bi-orthogonalization algorithms like Padé via Lanczos (PVL) [27, 28], or with methods based on orthogonalized Krylov subspace methods [29, 30, 31].

To generate a guaranteed passive reduced order model for (4) that matches the first q moments of the transfer function, one can use the PRIMA approach [31]. The first step of the approach is to use an Arnoldi algorithm to generate a set of $q+1$ orthogonal vectors, $\boldsymbol{V}_q$, that span the Krylov subspace

$$\boldsymbol{V}_q \in span\left\{\boldsymbol{D}, \boldsymbol{A}\boldsymbol{D}, \boldsymbol{A}^2\boldsymbol{D}, ..., \boldsymbol{A}^{q-1}\boldsymbol{D}\right\} \quad (5)$$

where $\boldsymbol{A} = \boldsymbol{\mathcal{R}^{-1}\mathcal{L}}$, and $\boldsymbol{D} = \boldsymbol{\mathcal{R}^{-1}B}$. Then the reduced-order model is

$$s\tilde{\mathcal{L}}\,\tilde{\boldsymbol{x}} = -\tilde{\mathcal{R}}\,\tilde{\boldsymbol{x}} + \tilde{\boldsymbol{B}}\,V_t \quad (6)$$

$$I_t = \tilde{\boldsymbol{B}}^T\tilde{\boldsymbol{x}}, \quad (7)$$

where $\tilde{\mathcal{L}} = \boldsymbol{V}_q^T\mathcal{L}\boldsymbol{V}_q$, $\tilde{\mathcal{R}} = \boldsymbol{V}_q^T\mathcal{R}\boldsymbol{V}_q$, $\tilde{B} = \boldsymbol{V}_q^T B$, and $\tilde{C} = \boldsymbol{V}_q^T C$.

5 Problems

Although the combination of integral formulations, sparsification and model-order reduction makes simulation of RLC effects in 3-D interconnect tractable, there are still a number of challenges. In the subsections below we describe three such challenges: handling the non-ideal semiconductor substrate, picking expansion points for model-order reduction, and handling the massively coupled problem.

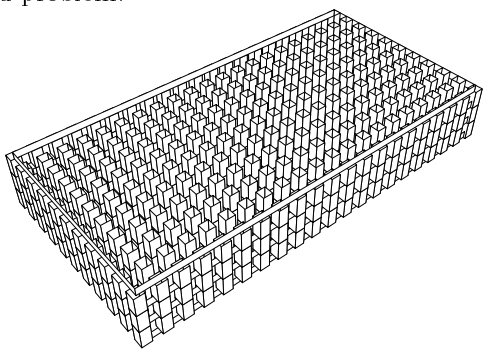

Figure 3: three dimensional discretization of the semiconductor substrate.

5.1 Substrate Discretization

One of the difficulties in using the discretized integral formulation in (4) for on-chip inductance computations is handling the far from perfectly conducting semiconductor substrate. Since current penetrates some tens of microns into the substrate [32], the substrate must be discretized as shown in Figure 3. This substrate discretization creates an enormous number of filaments, slowing even the fastest of sparsification techniques. For this reason, there has been renewed interest in developing purely surface formulations [33].

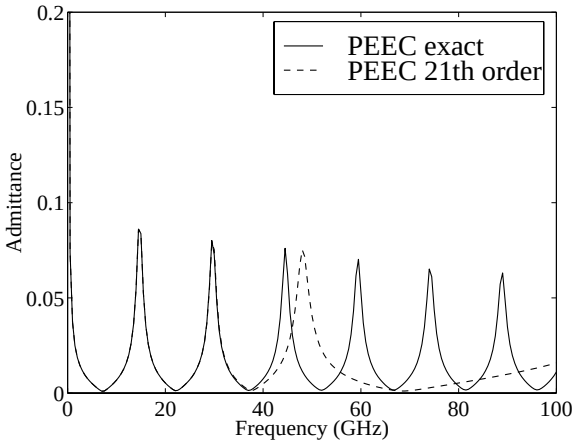

Figure 4: The response of the transmission line.

5.2 Multipoint Approximations

Model order reduction using $s = 0$ as an expansion point can become quite inefficient. To demonstrate this, the formulation and model-order reduction was applied to a 1 cm long transmission line example. The line was divided into 40 sections along its length, each section was divided into a 9 filament bundle, and each node had 12 panels leading to a 1704 element circuit. The line was shorted at the far end and the admittance was computed using both the full model and a 21st order reduced model. As Figure 4 shows, the reduced order model captures only a few resonances. This phenomenon can be explained by examining the pole locations of the original and reduced-order models, as shown in Figure 5. As is clear from the figure, the model-order reduction is "fooled" by inconsequential poles on the real axis. The most fruitful approach to addressing this problem is to use multipoint matching schemes [24, 34], which can be passivity preserving [35]. Although it is easy to select good expansion points for a given senario, the techniques for automatic expansion point selection are still far from optimal.

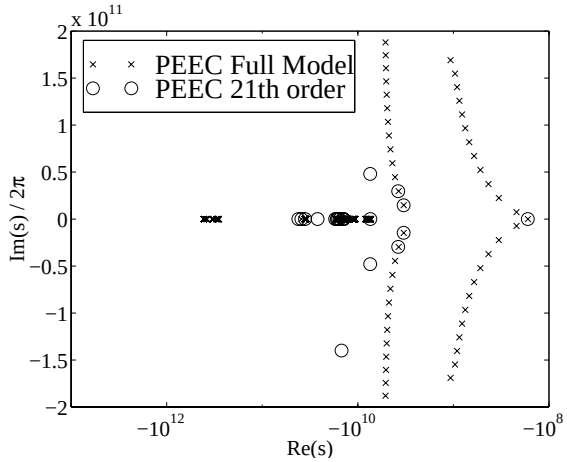

Figure 5: The poles of the transmission line.

5.3 Massively Coupled Problems

Interconnect problems with a small number of terminals can be handled using block model-order reduc-

tion methods, even though the reduced models represent the terminal interactions in a dense way. In an RF design, like the one in Figure 6, there may be electromagnetic coupling between each of thousands of interconnect lines. Representing those millions of interactions directly is computationally intractable.

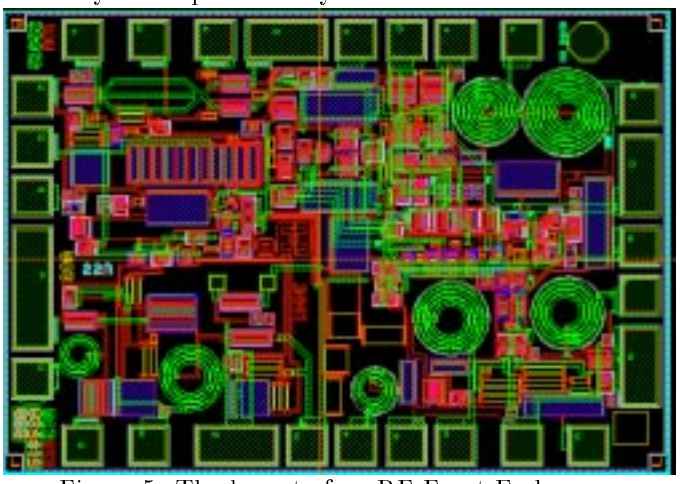

Figure 5: The layout of an RF Front End.

6 Conclusions

In this paper we briefly reviewed recent work on combining discretized integral formulations, sparsification techniques, and krylov-subspace based model-order reduction. We then described a few of the problems these new methods have uncovered.

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