Digital Detection of Analog Parametric Faults in SC Filters*

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Abstract

Many design for test techniques for analog circuits are ineffective at detecting multiple parametric faults because either their accuracy is poor, or the circuit is not tested in the configuration it is used in. We present a DFT scheme that offers the accuracy needed to test high-quality circuits. The DFT scheme is based on a circuit that digitally measures the ratio of a pair of capacitors. The circuit is used to completely characterize the transfer function of a switched capacitor circuit, which is usually determined by capacitor ratios. In our DFT scheme, capacitor ratios can be measured to within 0.01% accuracy, and filter parameters can be shown to be satisfied to within 0.1% accuracy. A filter can be shown to satisfy all its functional specifications through this characterization process. We believe the accuracy of our scheme is at least an order of magnitude greater than that offered by any other scheme reported in the literature.

1 Introduction

On-chip design for test (DFT) techniques have been suggested as one method to reduce test costs in analog and mixed-signal circuits [1]-[16]. A test process is judged by its cost and the quality of the product that passes the test process. Many DFT techniques suggested in the literature for analog circuits have been shown to be effective at detecting locally catastrophic faults. That is, faults which cause significant variations in the value of a single component. The validation has been both through circuit simulation and through the fabrication of test ICs with artificial fault injection. In analog circuits, parametric or "soft" faults, that is minor component variations, are as important as catastrophic faults. However, the studies of the ability of DFT schemes to detect parametric faults have been very limited.

Parametric faults occur due to normal variations in the manufacturing process and cause the values of one or more circuit components to deviate from their expected values [12, 13, 14]. For minor single component deviations, the deviation in the output from its expected value (caused by the component variation) may be acceptable. Thus, only large single component deviations may cause output errors. It is possible for a collection of minor variations in multiple components may cumulatively cause the output to be erroneous. Unfortunately, not every possible set of variations is guaranteed to cause an output error and therefore, not every multiple component variation is actually a multiple parametric fault. Only those multiple deviations that actually cause output errors are parametric or soft faults. To further complicate matters, errors in the outputs are defined by circuit specifications. A multiple component variation that corresponds to a fault in one application may result in acceptable variations for another application. Since the number of potential parametric faults is infinite the fault coverage for multiple parametric faults cannot be judged by fabricating a small number of ICs, or by simulating a small number of faults. It can be shown that adequate fault coverage can only be guaranteed with high accuracy signal measurement.

Contributions We present a DFT scheme for switched-capacitor circuits that realizes the required high measurement accuracy. We develop a circuit, an *analog-to-digital capacitor ratio converter (ADCRC)* which given two capacitors C_1 and C_2 produces a digital estimate of the ratio $\frac{C_1}{C_2}$. The accuracy of the digital estimate can be as high as 15 bits. In other words, the ratio can be estimated to better than 0.01%. The functionality of a switched-capacitor filter is determined primarily by a number of capacitor ratios. The ADCRC circuit can be used to accurately compute *all* the capacitor ratios that determine the transfer function of the filter. In other words, *the DFT scheme can completely characterize the functionality of the filter*. This characterization can be used to determine if the filter that has been realized satisfies its specifications. This approach offers a number of advantages:

- Each ratio is measured on-chip in the digital domain, with an accuracy at least an order of magnitude greater than that reported by previous on-chip test techniques.
- Functional test and self-test techniques have to verify *all* of a filter's specifications. In the absence of reliable system models, the results from some functional tests cannot be used to deduce the ability of the system to meet other specifications. By characterizing the transfer function, we verify *all possible* specifications.
- The technique can be implemented in manner that is consistent with the design practices used for switched capacitor analog circuits.

2 Previous Work

Most DFT schemes for analog circuits aim to reduce test generation difficulties and improve fault coverage. Some DFT schemes

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are extensions of techniques developed for digital circuits. However, the test difficulties experienced with analog and mixed-signal circuits are significantly different from those associated with digital circuits. For example, accurate signal measurement is far more difficult in analog circuits[1]. Thus, many DFT schemes exploit characteristics unique to analog circuits, such as regularity in circuit structure and/or relationships between on-chip signals, and target test problems unique to analog circuits. All DFT schemes require the addition of hardware for switching circuitry and functional elements. In addition, many schemes are limited in their application to specific circuit macros such as data converters or filters. Macro-specific DFT techniques reported in the literature fall into one of the following categories:

Reconfiguration for test : Reconfiguration-based test methods require the addition of a switching network, and the creation of a test mode in which the circuit is reconfigurable [2]-[5]. Reconfiguration has been used to improve testability in analog and mixed-signal circuits in two ways. We refer to one type as reconfiguration for access. The basic approach is similar to one used for digital circuits. The circuit to be tested is partitioned into several blocks such that the inputs to and the outputs from each block can be directly controlled and observed. The details of the application of reconfiguration for access are circuit specific. Reconfiguration simply increases access to the circuit components, without altering them.

The second type of reconfiguration-based DFT technique is an indirect approach to testing that is unique to analog circuits. We refer to this technique as reconfiguration for redesign. Reconfiguration is used to rearrange the components to form an easily testable circuit. The response of the altered circuit, in its easily testable configuration, is used as a guide to determine if the original circuit, in its normal configuration, will work. Unlike circuit-specific reconfiguration for access techniques, almost all the reconfiguration for redesign techniques discussed in the literature have been macro-specific.

Code-based test : This approach is based on methods used to design on-line error detection schemes for fault-tolerant digital systems [7-13]. Code-based techniques target the difficulty encountered in measuring the values of on-chip signals. A redundant data code is used to encode on-chip data. On-chip code checkers, rather than off-chip instrumentation, are used to verify that the data code is not corrupted. Faults are detected indirectly such that those that corrupt the code are the only ones that are flagged by the checkers. To limit the number of faults that escape detection and to obtain a high fault coverage, the circuit can be redesigned to improve the number of faults that corrupt the data code. The code used most commonly is the data duplication code.

Two previous efforts are directly relevant to the method discussed in this paper. The technique in [5] also measures individual capacitor ratios to characterize the quality of a realized filter. Capacitor ratios are measured by configuring the pair of capacitors whose ratio is to be measured as a voltage follower. The power supply voltage is used as the input voltage to the voltage follower. However, this interesting technique suffers from two significant limitations:

- The variations in the supply voltage which can be as high as 5% limit the accuracy with which ratios can be measured.
- Fast accurate off-chip measurement techniques are needed to accurately measure the output of the voltage follower.

A functional self-test technique based on using digital circuitry to generate functional test signals has been extensively investigated [19]. This technique also achieves substantial accuracy by moving analog signal measurement to the digital domain. However, one limitation of any functional test technique is that the functionality of the filter can only be guaranteed if all the specifications have been tested for. In the absence of suitable models, one cannot make make general deductions about the ability of a circuit to satisfy all its functional specifications by testing for only a few of them.

3 Analysis

First, we discuss the impact of process variations on circuit elements and outputs. Next, we examine the ability of the DFT techniques reported in the literature to detect multiple parametric faults.

3.1 Process Variations

With any process, the actual realized values of circuit components will differ from the expected or the desired values. Across several ICs, for the same design, the realized values will typically be both greater than and less than the expected nominal values. Process statistics can be used to estimate the expected range of variation in the value of each on-chip component. Random variables are commonly used to represent and analyze the impact of process variations. As do others, we use Gaussian distributions [17] to model the impact of process variations on component values.

Components In integrated circuits, though the absolute values of on-chip components can vary significantly from their expected values, relative matching between components is high [14,15]. Thus, most analog ICs use the relative matching between physically similar components to set circuit parameters. Several examples of such circuits have been discussed in this chapter. When ratios are used to set transfer functions, output parameters are immune (as a first order approximation) to shifts in the mean values of components. Only relative shifts between components are of importance. Correspondingly, for our purposes, we need not model absolute variations in components. Thus, we will only model relative shifts in component values. On-chip components will be modeled by Gaussian variables centered around a fixed mean. The statistics of the distribution is determined by the fabrication process.

Outputs In general, the output of an analog circuit is a nonlinear function of the component values. It would appear to be difficult to compute the output distribution from the component distributions. However, because the component variations of interest are small, at a given test point, the transfer function with respect to component values can be linearized using sensitivity analysis [16]. The linear sum of several Gaussian distributions is also a Gaussian distribution [15]. Thus, about each test point the variations in the output value can be modeled as a Gaussian distribution about a zero mean.

Signal Tolerances At each test point, a range of output values is defined as being acceptable. The output tolerance Do is the accepted variation in the output at a test point. The output tolerance is defined by the specifications, measurement tolerances and the expected impact of process variations. Thus, the value of signal $x1$ is acceptable if $-Do < x_1 < Do$. The output tolerance will be circuit and test-point specific. Similar tolerances will have to be allowed in test points in a circuit reconfigured for redesign and in code checkers used to monitor on-chip signals.

3.2 Performance Metrics

In this section, we define some terms to enable us to quantify values of interest.A good IC is one for which all outputs are at their

expected values within tolerances. In a real test process, some good units will fail the test, and some bad units will pass the test. Probabilistic or statistical analysis is the only practical method to assess the parametric fault coverage of a test process. Let PG be the probability of manufacturing a good IC. PB = 1 - PG is the probability of manufacturing a faulty IC. An ideal test process will pass all good ICs and fail all bad ICs. Some, but not all, of the following terms, or terms similar to those listed below, have been previously defined [14]. The effort in [14] develops methods to reduce test time in analog circuits. We reuse these definitions in the context of design for test.

The following terms categorize good and faulty units with respect to their performance on the test process:

1. PGP is the probability that a good IC will pass the test.
2. PGF is the probability that a good IC will fail the test.
3. PBP is the probability that a bad IC will pass the test.
4. PBF is the probability that a bad IC will fail the test.

The fault coverage of the test process is F = PBF/PB. The yield is Y = PGP/PG.

3.3 Simulation Results

In a Monte-Carlo analysis scheme, the target circuit is simulated N times using a standard circuit simulator. Process statistics are used to model the range and pattern of variations in component values for each of the components in the circuit. On each iteration, the circuit is simulated with a different set of component values. The simulation is used to determine if the circuit is good or bad and if it passes/fails the test process. The results of the simulation are used to estimate the fault coverage and the yield. We have developed a parametric fault-effect analysis tool (pFEAT) for switched-capacitor circuits. pFEAT uses the SWITCAP format as the input, and uses it as the circuit simulator. Our tool pFEAT is used to simulate the impact of process variations on the passive components, and their consequent impact on circuit functionality. The tool can be used to evaluate both code-based and reconfiguration-based DFT schemes.

Performance Comparison Statistical experiments using pFEAT were conducted for a wide range of analog DFT schemes reported in the literature. The results of the experiments are summarized in Table 1. For brevity, we present only a summary. For each scheme, the threshold (for the checker or the test point in the reconfigured circuit) was set such that the yield of the test process would be approximately 90%. All the schemes were simulated assuming the probability of manufacturing a good unit, PG = 0.9. For each scheme, we report the best achieved combination of fault coverage and yield. As can be seen, some schemes are more effective than others. Yet, the fault coverage is generally very disappointing. None of the fault coverages listed would be acceptable for digital circuits.

3.4 Measurement Accuracy

Both approaches to DFT are adversely affected by one significant factor: process variations have the same impact on signals in the test mode and during normal operation. In general, to measure a signal, the measuring instrument should be of greater accuracy than the signal being measured. The same should be true of DFT schemes. Signals in the test mode should have an accuracy greater than that of signals during normal operation. Consider the duplication-code based DFT scheme. Process variations will cause the same range of variations in all the components of the code. We will refer to one of the two signals as the "original," and the second

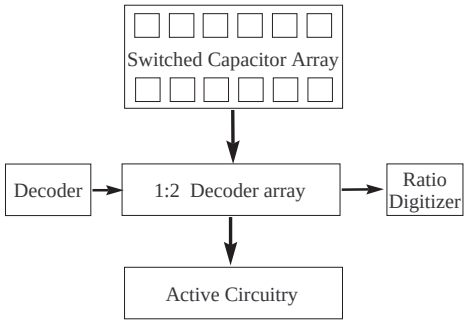

Figure 1: Block diagram for proposed DFT scheme

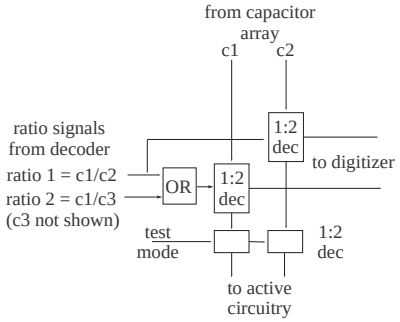

Figure 2: Reconfiguration network for proposed DFT scheme

as the "check" signal. If, for the check signal, the impact of process variations could be reduced its accuracy would be greater. The actual value of the check signal will be close to its expected value in spite of process variations. The more accurate signal will serve as a reference signal for the second signal in the code. Thus, the fault coverage and the success rate of the DFT scheme can be improved.

4 DFT Scheme Structure

We obtain accuracy by digitally estimating capacitor ratios. The ratio digitizer DFT scheme proposed in this paper can be systematically implemented using a procedure compatible with design techniques for switched capacitor filter circuits. As mentioned earlier, most capacitors in a circuit are defined as multiples of a unit capacitor. In SC circuits, all the capacitors required for the design are realized together in a single two-dimensional physical array of unit capacitors. Each capacitor required in the design is formed by electrically connecting the appropriate number of unit capacitors. The array contains enough unit capacitors to form all the capacitors required by the design. The sizes of a few elements in the array may be a fraction of the unit size to accommodate non-integer ratios. There are two outputs (one for each terminal) for each capacitor realized.

At the system level, the DFT scheme can be realized as shown in Figure 1. The test process is executed in several iterations. On each iteration, the digitzer (ADCRC) verifies the accuracy of one ratio, a process that requires multiple clock cycles. Figure 2 shows how the outputs of a pair of capacitors, whose ratio is to be measured, are directed to the inputs to the ratio digitizer. At the system level, as shown in Figure 1, on each iteration a decoder (similar to a memory address row decoder), is used to select a signal which the drives a pair-level decoder structure shown in Figure 2. The test mode signal isolates the capacitor array from the active circuitry

DFT Test Method	Authors	Type of circuit	Yield	Fault Coverage	Optimal m
Code-based	Direct duplication [11]	2nd order lowpass filter	0.916	0.566	1.1
	Pseudoduplication [9]	Lossy integrator	0.900	0.209	1.6
	Fully differential [6]	2nd order low pass filter	0.918	0.081	1.9
	Checksum coding [10]	2nd order low pass filter	0.900	0.350	1.5
Reconfiguration-based	TF re-evaluation [8]	2nd order low pass filter	0.911	0.659	1.4
	Signal propagation [7]	3rd order low pass	0.918	0.121	1.7
	Oscillation [2]	2nd order low pass filter	1.000	(0.62) 0.008	(0.38) 1.2

Table 1: Performance Comparison

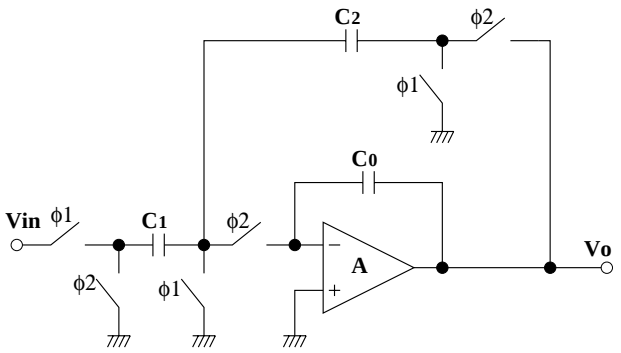

Figure 3: Simple lossy integrator circuit diagram

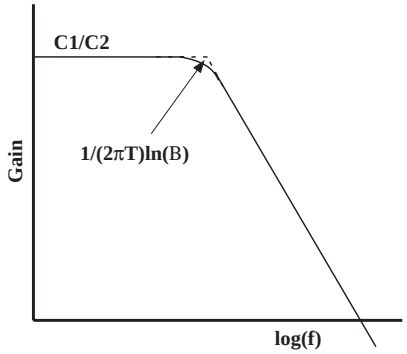

Figure 4: Transfer function for lossy integrator

during the test process. No more than one output of the decoder is active at any instant. The system-level decoder has as many outputs as there are ratios to be measured. If a capacitor belongs to multiple ratios, it has to be connected to more than output of the system-level decoder. These signals are ORed as shown in Figure 2. In the figure c1 is used in two ratios, whereas c2 is used in only one ratio. The configuration shown in Figures 1 and 2 offers two primary advantages:

- The test structure introduces additional parasitics at the outputs of the capacitors. However, the additional capacitive load on all the capacitors is minimized. All capacitors see the same type of load. Hence, the additional load can be characterized with minimal effort. The size of the load can also be tuned to each capacitor, by increasing transistor sizes in the 1:2 decoders, to make the additional parasitics proportional to the sizes of each of the capacitors
- The design process for this DFT scheme is very simple. Methods to systematically design decoder structures are well-known.

5 DFT Scheme Implementation

Our DFT technique targets the functional performance of switched-capacitor (SC) circuits. In particular, we concentrate on SC filter circuits. To illustrate our methodology by way of a simple example. These are followed by results for more complex designs.

5.1 Lossy integrator example

Consider the SC lossy integrator circuit shown in Figure 3. The transfer function for the filter is given by equation 1. For simplicity, we shall currently limit ourselves to ideal amplifiers.

$$\begin{aligned} H(z) &= \frac{C_1}{C_o+C_2}\,\frac{z^{-1}}{1-\frac{C_o}{C_o+C_2}z^{-1}} \\ &= \frac{\alpha\, z^{-1}}{1-\beta\, z^{-1}} \end{aligned} \qquad (1)$$

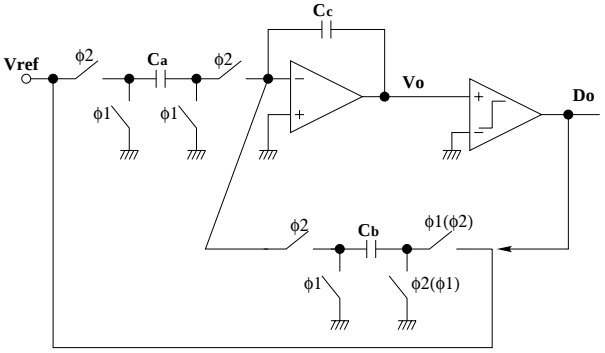

Figure 5: Analog-to-digital capacitor ratio converter

where $\beta = \frac{1}{1+\frac{C_2}{C_o}}$ provides the pole location on the z-plane and $\frac{\alpha}{1-\beta} = \frac{C_1}{C_2}$ provides the magnitude of the transfer function at DC. The transfer function for this circuit is plotted in Figure 4

We note that both the pole location and the DC gain are a function of capacitor ratios. Therefore, if we can accurately measure the ratio of capacitors we can provide information about the functional performance of the switched-capacitor filter. In particular, for our example if we obtain the capacitors ratios C_2/C_o and C_1/C_2 we have effectively "tested" the functional performance of this SC lowpass filter. We use an ADCRC circuit, that is explained next, to obtain the capacitor ratios.

ADCRC Figure 5 shows the circuit diagram for an analog-to-digital capacitor ratio converter (ADCRC). This circuit is able to accurately converter a capacitor ratio into a digital value. It can be shown that the voltage at the output of the integrator, $V_o(n)$, after n clock cycles is given by equation 2 [18].

$$V_o(n) = \frac{C_a}{C_c}\, n\, V_{ref} - \frac{C_b}{C_c} \sum_{i=0}^{n-1} Do(i)\;\; V_{ref} + V_o(0) \qquad (2)$$

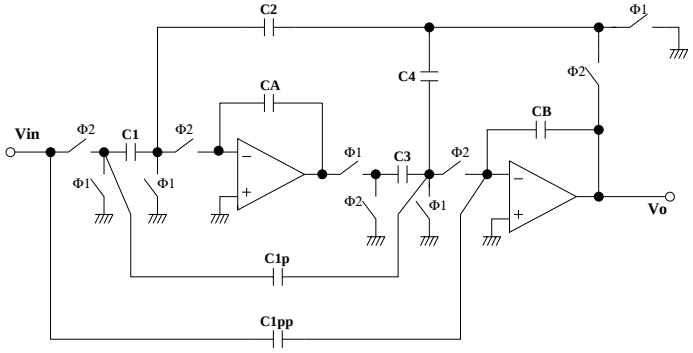

Figure 6: Low Q switched-capacitor biquad circuit

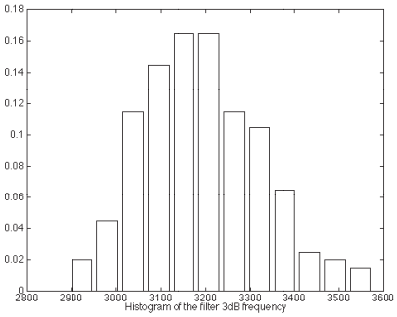

Figure 7: Histogram of the variation in the 3dB frequency of the SC lowpass filter

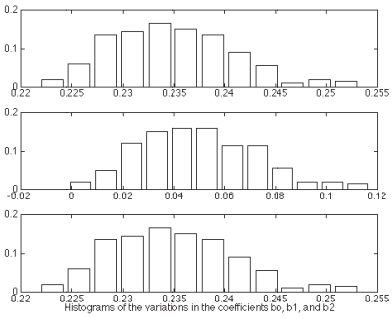

Figure 8: Variation in the numerator coefficients

With appropriate algebraic manipulation it can be shown that the average digital value of the output is given by equation 3. Note that the two values of the digital output are $+1$ and -1 and n is the number of iterations for conversion.

$$V_{digital-average} = \frac{1}{n}\sum_{i=0}^{n-1} Do(i) = \frac{C_a}{C_b} - \varepsilon_n \tag{3}$$

where

$$\varepsilon_n = \frac{1}{n}\left[\frac{V_o(n) - V_o(0)}{V_{ref}}\right]\frac{C_c}{C_b}$$

Further, it can be shown that the worst case error is given by

$$\varepsilon_{n_{max}} = \frac{2}{n}\left[1 + \frac{C_a}{C_b}\right]$$

The set of equations above are valid for $C_a \leq C_b$, with the result the error can always be bounded by $4/n$ and can be made extremely small by increasing the value of n, i.e., the time spent on converting the capacitor ratio into a digital format. The capacitor ratios of interest for our simple lossy integrator are C_1/C_2 and C_2/C_o. We can obtain both these values by connecting the appropriate capacitors to our ADCRC circuit shown in Figure 5. In our simple example the relationship between the functional performance and the capacitor ratios were fairly straight forward. However, as illustrated next the relationship is somewhat more complex for even moderately complex circuits. So, one has to resort to numerical techniques rather than closed form solutions.

5.2 Switched-capacitor biquad example

Figure 6 [17] shows the circuit diagram for a low Q switched-capacitor biquad filter section. The transfer function for a lowpass version of this circuit can be shown to be given by equation 4. We note that both the pole radius and angles are functions of capacitor ratios only.

$$H(z) = \frac{\frac{C_1C_3}{C_a(C_b+C_4)}z^{-1}}{1 - \frac{2C_aC_b+C_aC_4-C_2C_3}{C_a(C_b+C_4)}z^{-1} + \frac{C_b}{C_b+C_4z^{-2}}} \tag{4}$$

where the radius of the pole locations on z-plane is given by equation 5 and the angle of poles is given by equation 6.

$$r^2 = \frac{1}{1+\frac{C_4}{C_b}} \tag{5}$$

$$\theta = cos^{-1}\left[1 + \frac{C_4}{2C_b} - \frac{C_2C_3}{2C_aC_b}\right] \tag{6}$$

Equation 4can be rewritten in the form shown in equation 7.

$$H(z) = \frac{b_o + b_1z^{-1} + b_2z^{-2}}{a_o + a_1z^{-1} + a_2z^{-2}} \tag{7}$$

In general, functional specifications place limits on the range of variations in measurable output parameters. For example, in the case of a SC lowpass filter the list of functional specifications include the DC gain, the 3dB bandwidth, the in-band ripple, the out-of-bad attenuation, etc. In the next set of graphs we show numerical results of how the constraints on the output performance specifications for a 2nd order SC lowpass filter may be translated into the specifications on the range of variations on the capacitance ratios. The first, Figure 7 shows the variation in the 3dB frequency of the SC lowpass filter. This variation in the 3dB frequency is then translated into variations in coefficients of the z-domain transfer function shown in equation 7. The variations in the coefficients are shown in Figures 8 and 9

For our simple lossy integrator the translation from functional performance was relatively straight forward. As seen for the low biquad this is not always the case. However, once the limits for the coefficients of the transfer function are obtained, as shown in Figures 8 and 9, the corresponding range of values for the capacitor ratios can be obtained. If the coefficients of the transfer function are only a function of a single capacitor ratio, as is pole radius in equation 5, then the translation of the range of values for the coefficients of the transfer function to range of values for the capacitor ratios is fairly straight forward. In general, capacitor ratio matching is a function of the capacitor size as well as the desired capacitor ratio. If the coefficient in question is a product of N ratios then each capacitor ratio needs to be better controlled. In particular, if we first assume that the matching of capacitor ratios is constant then range

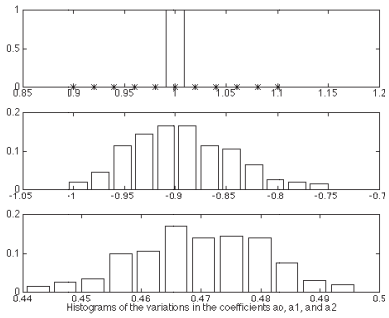

Figure 9: Variation in the denominator coefficients

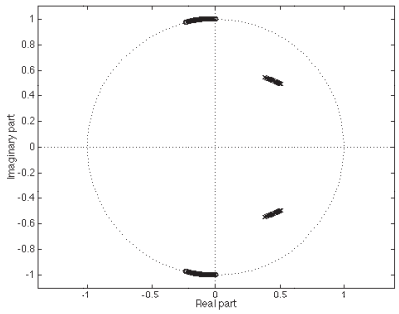

Figure 10: Variations in the pole and zero location in the z-plane

of values for the capacitor ratios needs to be matched to Nth root of the coefficient. Similar expressions can be developed for more complex functions.

In theory, from equation 3 the capacitor ratio can be measured to arbitrary precision. However, this is limited by device noise, clock feedthrough, finite gain and bandwidth and other analog considerations. However, obtaining 12 to 15 bits of resolution in the ratio precision is definitely possible. With the result that the proposed DFT scheme is extremely effective. Because the final limits of this process are not easily quantifiable, results from circuit simulation are not likely to prove too conclusive. However, to ensure the validity of our approach we ran a Monte-Carlo simulation on the lossy integrator circuit using Matlab. During each run the capacitor ratios had a one sigma deviation of 1%. Each capacitor ratio was measured with a 12-bit accuracy (requiring 2^{12} clock cycles). Starting with a initial yield of 86.6 the parametric fault coverage was 99.8% and the yield loss was 0.4%.

6 Conclusions

We present a DFT scheme for switched-capacitor circuits that realizes extremely high measurement accuracy. Relative to other techniques reported in the literature, our technique offers several advantages and disadvantages.

We believe the accuracy of our technique is at least an order of magnitude greater, if not more, than that of any design for test scheme reported in the literature. Code-based DFT schemes suffer from the limitation that the signals cannot be measured with an accuracy greater than the tolerance desired in the signal. Reconfiguration-based DFT schemes suffer from the limitation that the circuit tested is not the one used. The reconfigured circuits are not characterized completely but only tested to see if they meet a different set of specifications. It can be shown that even if the reconfigured circuit meets all its specifications, only conclusions of limited utility can be drawn about the quality of the original circuit.

As in [5], we too test a filter by completely characterizing all capacitor ratios of interest. We are able to achieve accuracy far greater than that reported in [5] by moving ratio estimation to the digital domain. Further the accuracy of the estimate is not significantly influenced by the tolerance of any reference signal. By accurately characterizing all capacitor ratios of interest, we are able to characterize the transfer function of the filter. Therefore, we are able to verify the ability of the filter to satisfy all its specifications, and the tolerance achieved in each of these specifications.

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