PANEL:
Cell Libraries Build vs. Buy; Static vs. Dynamic

Chair: Kurt Keutzer, Univ. of California at Berkeley, Berkeley, CA
Organizer: Emil Girczyc, Consultant, Los Altos, CA

Cell libraries determine the final density, performance, and power of most IC designs much as the construction materials determine the quality of a building. Nevertheless, the importance of libraries has often been a tertiary consideration in design projects - falling behind both design skill and tool quality. Choosing the right cell library for your project can have a significant impact on the characteristics of the circuit you design, and thus, the success of your product. Design teams need to consider a host of technical and business factors when selecting a library. Technical considerations include density, speed, power, design for reliability, and support for the designer's tools and flow. Business considerations include price, risk, time to market, and control of one's own destiny.

This panel examines technical, as well as current business issues, associated with cell libraries. On the technical front, the advantages and disadvantages of static libraries versus ``on the fly'' or dynamic libraries will be discussed and quantified. On the business front, while designers have traditionally used the cell libraries provided by their silicon source (internal division or semiconductor vendor), recent changes in technology and business practices make several cell-library sources available to design groups: silicon vendors, third party library vendors, and internally created. This panel will explore the business issues associated with the library choice and debate when designers should use each available source of cell libraries.

Kurt Wolf, Director, Library Services,
TSMC, San Jose, CA

The third party foundation cell library industry exists because of the technical and economic benefits of specialization that is driven by very deep sub-micron process technologies. However, not all cell libraries are equal. Alignment of goals across designers, library vendors, and foundries, is essential to successful completion of chip designs.

Different circuit design projects are best served by different cell libraries – each representing a different speed, area, risk, and cost tradeoff. Design groups are best served by picking the library that best meets their needs. Foundries are working closely with third party library companies to insure that these libraries work reliably on the foundry's process. Foundries, third party library companies, and circuit design companies are also cooperating to create business models that fairly represent the value contributed by each party. Designers can choose from a combination of parameters that include density, high speed, ultra low power, library & tool integration, and special cell development.

David Pietromonaco, ASIC Library Project Manager,
Hewlett Packard, Palo Alto, CA

As companies integrate more and more of their systems on a chip, ASIC design must support the entire system design process, from initial design, through to debugging. By tightly coupling our own fabs with our silicon verification and our libraries, we can cut guardbanding and achieve the most efficient use of silicon area while making the design and debug cycle easier. By using automated library generation techniques, we can now affordably create multiple libraries tailored for specific purposes (such as high speed, high density, low power, etc.) that can be mixed and matched to create the specific IP blocks we provide as well as the designers' custom circuitry.

DAC 99, New Orleans, Louisiana

Jay Maxey, SMTS, ASIC Product Development,
Texas Instruments, Dallas, TX

Silicon vendors have a vested interest in insuring that customers can effectively and reliably build chips using their silicon processes. An advantage inherent to an integrated ASIC supplier such as TI is the synergy amongst library developers and fab engineers which can be leveraged to provide libraries and design flows tailored to advanced processes capability at the earliest opportunity.

At TI, highly automated cell-create flows in concert with specialized circuit design expertise provide the cornerstone of our approach to ASIC library development. Our approach places strong emphasis on quality while at the same time facilitating throughput in both development and delivery.

Jeff Lewis, VP of Marketing,
Artisan Components, Sunnyvale, CA

Physical libraries-standard cells, embedded memories, and I/O cells- are the foundation upon which most of the world's silicon is built. More than any EDA tool, libraries determine the speed, power, and density of the resulting silicon. Developing a mediocre library is easy, but developing a library that can achieve the performance, quality, and EDA tool integration that IC designers expect has become a very specialized task. Commercial library suppliers can build differentiated products because they can spread the requisite investment across dozens of library deliveries each year, enabling them to invest in (1) fundamental, patented technology, (2) a broad portfolio of EDA tools for library development and integration testing, (3) a world-class group of library specialists, and (4) rigorous development and validation methodologies. Because of specialization, focus, and investment, commercial libraries are the lowest risk, lowest cost library alternative available today.

Martin Lefebvre, President and CEO,
Cadabra Design Technology, Santa Clara, CA

IC designers of the deep submicron era face several new challenges that directly impact library development strategies. Salient among these challenges is the need to tune transistor netlists and sizes for optimal performance and power dissipation, as well as the need to support qualitative process differences when targeting multiple foundries. Design teams that develop their own libraries best meet these challenges, and with automated transistor layout, design teams are able to exploit untapped opportunities in potential area, speed, and power optimization. Internally developed libraries also offer powerful business advantages: reduced manufacturing costs, increased product competitiveness, reduced time-to-market for new fabs, and the flexibility to access the fab of your choice.

Jeff Burns, Research Staff Member,
IBM Austin Research Lab, Austin, TX

Cell-based layout methods, based on pre-designed libraries, are widely used to realize random logic for ASIC and microprocessor designs. However, in high-performance applications, the use of fixed, pre-defined cell libraries is becoming increasingly unattractive. Fixed libraries preclude tuning device sizes for delay and power optimization. Adding new cells to a library, to support functions or electrical requirements not foreseen by the library designers, is often cumbersome or impossible in fixed-library methodologies. The physical characteristics any given library (cell height, maximum FET finger size, etc.) are seldom optimal for all applications of interest, even within a single chip. The solution to these difficulties is the use of on-the-fly cell generation. Cell generation for static CMOS random logic has matured to the extent that production, high-end microprocessors have been successfully build using on-the-fly generation. As CMOS technology matures and competitive pressures increase, the need to adopt on-the-fly cell generation will grow.