

# An Efficient Structural Approach to Board Interconnect Diagnosis

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## Abstract

*This paper presents a new structural approach for diagnosing board interconnects using boundary-scan. While existing diagnosis approaches assume only wired-AND or wired-OR bridging fault model, we consider a more complex bridging short fault model in CMOS circuit environment. The diagnostic test set is generated based on graph theoretic technique and the adjacency fault model is adopted. Both one-step and two-step diagnosis algorithms are given. They guarantee the complete diagnosis of multiple interconnect faults with no aliasing and confounding. The algorithms have been evaluated by simulation on several benchmark layouts and randomly generated layouts. Simulation results show that more than 50% reduction in the number of tests can be achieved for two-step diagnosis when the fault rate is very small, such as in a matured product line. This can significantly save the diagnosis cost for boundary-scan testing.*

## 1 Introduction

The packaging density of a printed circuit board (PCB) or multichip module (MCM) has been increasing due to the miniaturization of digital circuits and current technologies. With such a high density and complexity, shorts are more likely to happen among interconnect nets. As a result, testing and diagnosis for interconnect faults is an important problem in VLSI, PCB and MCM manufacturing. In general, there are three types of faults commonly associated with nets on a PCB. They are stuck-at-faults, open faults, and bridging faults. In all cases, all nets involved in a short will have the same resulting logic value.

With IEEE Std 1149.1 boundary-scan architecture [1], these interconnect faults can be tested and diagnosed under full controllability and observability conditions. In a boundary-scan environment, test sets are scanned in, the saving in the number of tests and the test application time is particular important. A variety of approaches [2]-[10] has been proposed for generating diagnostic test sets based on boundary-scan architecture. They differ with each other in their diagnostic resolution. In general, these approaches fall in two basic categories: the *behavioral testing* and the *structural testing* strategy. It is important to note that the previous diagnosis approaches assume only wired-AND or wired-OR bridging fault model, no matter the fault involves two nets or multiple nets. However, in a CMOS circuit environment, the fault model for bridging faults is rather complex than the wired-OR or the wired-AND model [11]. This is because a shorted net may settle to an indeterminate voltage level which makes prediction of the resulting logic levels very difficult. Recently, a new '*n+1*' Algorithm [12] has been proposed to overcome this deficiency. It can completely diagnose any multiple interconnect faults, regardless of the type of bridging faults. The drawback of this method is the large number of test vectors. This problem is especially severe if boundary-scan testing is employed, in which each parallel test vector has to be serially scanned into the board under test, resulting in a total test time of  $n \times (n+1)$ , where  $n$  is the number of nets.

In this paper, we propose a new structural diagnostic approach for board interconnect testing with boundary-scan. This approach not only tackles multiple faults, but also deals with more complex issues such as CMOS bridging faults. The test set is generated by a simple yet effective one-step diagnosis algorithm based on graph theoretic technique. The adjacency fault model in which two nets can be shorted only if they terminate at adjacent pins or their tracks are adjacent within a predetermined distance, is adopted [7]. A two-step algorithm is further proposed for test generation and diagnosis. Compared with one-step diagnosis, the two-step diagnosis algorithm can further reduce the number of test vectors while retaining the same level of diagnostic resolution. Both algorithms guarantee the complete diagnosis of multiple interconnect faults with no aliasing and confounding. Simulation results for benchmark layouts and randomly generated layouts show a 18% to 45% savings in the number of tests for one-step diagnosis. For two-step diagnosis, more than 50% reduction in the test length can be achieved when the short fault rate is very small. We shall also show the adjacency fault model has a major impact on the efficiency of the two-step diagnosis.

## 2 Preliminaries

This section will first give the basic definitions and notation. **Parallel Test Vector (PTV)**: the vector applied to all nets of a wiring network in parallel. **Sequential Test Vector (STV)**: the vector applied to a net, over a period time, by a sequence of PTVs. **Test Set S**: the collection of all STVs. Each column of S is a PTV and each row of S is a STV. **Sequential Respond Vector (SRV)**: the response of a net to a STV. **Syndrome**: the SRV of a faulty net. **Aliasing syndrome**: if a syndrome in the presence of a fault is the same as the fault free response of a net, then it is impossible to determine whether or not this net is also part of the short. The response in this case is referred to as an aliasing syndrome. **Confounding syndrome**: the bridge fault between a pair of nets may produce the same syndrome as between another net pair, so it is impossible to determine whether or not there is a short between which pair of nets. The response is called a confounding syndrome.

Given the layout of nets and the criteria for the short faults, the structure of the interconnect can be modeled by using an **adjacency graph**  $G_{ad}$  to reflect all the possible faults under consideration. The adjacency graph is given by  $G_{ad}=(V,E)$ , where each node in the set  $V$  identifies a net and an edge  $e_{ij} \in E$  if a short can exist between  $n_i$  and  $n_j$  as they are adjacent in the layout of the interconnect [13]. For each node  $v \in V$ , its **degree** with respect to  $G_{ad}$  is defined to be the number of other nodes adjacent to it in  $G_{ad}$ . Let  $D$  be the maximum degree of the nodes in  $G_{ad}$ . The **edge-distance** between two nodes in  $G_{ad}$  is the number of edges on the shortest edge path between the two nodes. A *k-coloring* of an arbitrary graph  $G_{ad}=(V,E)$  is a mapping  $f:V \rightarrow \{C_1, C_2, \dots, C_k\}$  which assigns a **color**  $C_i$  to each node in such a way that no two adjacent nodes receive the same color [14]. A *primary net* is defined as the particular net under consideration, while **Primary Shorting Nets (PSNs)** are the nets which are likely to be shorted to the *primary net*, i.e., for a node  $n_i$  in

$G_{ad}$  all the nodes  $n_j$  such that  $e_{ij} \in E$ . The set of **Secondary Shorting Nets (SSNs)** is defined as the primary shorting nets to the PSNs, but excluding the *primary net* itself.

The bridging short fault model under consideration is summarized as follows. For a given short fault, if the number of nets driving a logic 1 is larger than that driving a logic 0, then logic 1 dominates. Similarly, if the number of nets driving a logic 0 is larger than that driving a logic 1, then logic 0 dominates. As a matter of fact, this assumption is valid for most of the CMOS circuits. In the case where half of the shorted nets driving a logic 1 and the other half driving a logic 0, it reduces to a wired-AND short fault model. It is also assumed that both open and short faults do not exist on the same net.

### 3 One-step Diagnosis

The basic idea behind the one-step diagnosis algorithm is to reduce the number of test vectors by exploiting the net adjacency relationships in the layout. Unlike the conventional graph coloring problem [8]-[10], [14], where each node is assigned a color in such a way that no two adjacent nodes receive the same color, we made the problem more restricted in our algorithm in order to diagnosis all the multiple interconnect faults under our fault model.

Basically, the algorithm utilizes the test set from the ‘ $n+1$ ’ algorithm [12]. Instead of using  $n+1$  PTVs, the number of PTVs can be reduced to  $k+1$ , where  $k$  is the number of colors used when our algorithm is applied to  $G_{ad}$  and  $k$  is generally less than  $n$ . Each color  $C_i$  is first associated with a unique  $k+1$  bits STV  $\{b_{k+1}, b_k, \dots, b_2, b_1\}$ , where  $b_j = 0$  when  $j \leq i$  and  $b_j = 1$  when  $j > i$ . As a consequence, the net with color  $C_1$  is assigned with a STV  $\{111\dots110\}$ , while the net with color  $C_k$  is assigned with a STV  $\{100\dots000\}$ , where  $C_k$  denotes the largest color to be assigned. The test set  $S$  will be equal to  $(STV_1, \dots, STV_n)^T$ . With this test set, all stuck-at-faults can be detected since all STVs are different and contain at least one *zero* and *one*. Open faults can also be detected as this test set includes PTVs with all *zeros* and all *ones*. In addition, every STV contains different number of ones with a covering relationship. We say net  $a$  covers net  $b$  if and only if the STV for net  $a$  contains *ones* wherever STV for net  $b$  has *ones*. In other words, net with a lower color covers net with a higher color. Due to this covering relationship, two important behaviors with respect to this test set are observed under our fault model.

First, if two nets are wired-AND shorted, the resulting fault syndrome will be the same as the STV of one of the faulty nets that assigned with the higher color. Suppose for  $k = 6$ , if net with  $C_2$  and net with  $C_5$  are shorted, then the SRV for both nets will be equal to  $\{1111100\} \cap \{1100000\}$ , where  $\cap$  denotes the wired-AND operation. As a result, the fault syndrome becomes  $\{1100000\}$ .

Second, for a short involving  $m$  nets,  $m > 2$ , if we have a list contains the colors of these  $m$  nets in ascending order, then the resulting fault syndrome will be the same as the STV of the net with the  $(\lfloor m/2 \rfloor + 1)$ th color in the list. For example, for  $k = 6$ , if nets with colors  $C_1, C_3$  and  $C_4$  are shorted, the syndrome becomes the STV of the net with the second color in the list (1 3 4) and is equal to  $\{1111000\}$ , i.e., the STV assigned to the net with  $C_3$ . Similarly, if nets with colors  $C_1, C_3, C_4$  and  $C_6$  are shorted, the color list is (1 3 4 6) and the syndrome will then become  $\{1110000\}$ .

Based on these two behaviors, we come up with the following two corollaries which form the basic elements in our algorithm.

**Corollary 1** For a graph  $G_{ad}$ , color  $C_1$  can be reassigned to a node which has at least an edge-distance of 3 from those nodes already assigned with  $C_1$  such that no syndrome equal to the STV assigned to the net with  $C_1$  exists.

**Proof:** Since any two nodes with  $C_1$  are separated by at least two other nodes with different colors, a short involving  $p$  ( $p \geq 2$ ) nodes

with  $C_1$  contains at least  $p$  other nodes with different colors. By the above test set behavior, no resulting syndrome is equal to the STV of net with  $C_1$ . Thus, no aliasing and confounding.

**Corollary 2** For a graph  $G_{ad}$ , color  $C_k$  (the largest assigned color) can be reassigned to a node which has at least an edge-distance of 4 from those nodes already assigned with  $C_k$  such that no syndrome equal to the STV assigned to net with  $C_k$  exists.

**Proof:** Since any two nodes with  $C_k$  are separated by at least three other nodes with different colors, a short involving  $q$  ( $q \geq 2$ ) nodes with  $C_k$  contains at least  $(q + 1)$  other nodes with different colors. By the above test set behavior, the resulting syndrome is not equal to the STV of net with  $C_k$ . Even in the case where there are only two nets short, each involving a node with  $C_k$ , aliasing and confounding do not exist since there always exists at least one node separating these sets of shorted nodes.

With these two corollaries, the number of colors used can be reduced by reassigning  $C_1$  and  $C_k$  to the nodes in  $G_{ad}$ . However, colors between the lowest and the highest color cannot be reassigned since it cannot guarantee aliasing and confounding free due to the complicated short fault model. In addition, although these two corollaries are sufficient for full diagnosis, they may not be necessary.

In some cases, there may be one set of nets which are not shorted to another set of nets under the adjacency fault model. Thus, it is necessary to find (if any) the disjoint graph component  $G_{ad}$  from the adjacency list. There are three phases in the one-step algorithm. Phase 1, 2 and 3 are repeated for each connected adjacency graph  $G_{ad}$  until all the nets are assigned with colors and the number of colors or test vectors is minimized. It is important to note that the one-step algorithm can also be applied when the wired-OR two nets short fault model is assumed, by taking the complement of the STVs in the above test set.

In Phase 1, the nodes in  $G_{ad}$  are sorted according to their *degrees*. The node with the highest degree will be first assigned with a color and Phase 1 will exit if all nodes have been assigned with colors. For each node, the algorithm will check all its PSNs (Primary Shorting Nets) and SSNs (Secondary Shorting Nets). A node is assigned with  $C_1$  if and only if its PSNs and SSNs are not already assigned with  $C_1$ . Otherwise, the next lowest color is assigned. With this assignment scheme, the edge-distance for every pair of nodes with  $C_1$  will be at least equal to 3 after Phase 1. This follows Corollary 1 and no aliasing and confounding exist. The time complexity of Phase 1 is  $O(n \times D + n \times D^2) = O(n \times D^2)$ .

The goal of Phase 2 is to reduce the number of colors by assigning each node originally with the highest color  $k$  to the next highest color  $k-1$ , but with the constraint that all the edge-distances between nodes with  $C_k$  and nodes with  $C_{k-1}$  should be at least equal to 4. If this condition fails, Phase 2 will exit. The edge-distance between such a pair of nodes is computed by the *breadth first search algorithm* for shortest path problem [14]. After each successful iteration, the number of colors used is reduced by one, while the number of nodes with the updated highest color  $k$  is increased by one. The time complexity of Phase 2 is  $O(m \times n^2)$ , where  $m$  is the total number of edges  $|E|$  in  $G_{ad}$ . In case where  $G_{ad}$  is a complete graph, the time complexity becomes  $O(n^4)$ . However,  $m \ll n(n-1)/2$  under our adjacency fault model since  $G_{ad}$  is relatively sparse as  $D \ll n$ .

The number of colors can be further reduced by going through Phase 3 of the algorithm. In Phase 3, the edge-distance between each node with color  $C_k$  and node with color other than  $C_1$  and  $C_{k-1}$ , say  $C_j$ , is computed.  $j$  is first selected to be  $k-2$ . If all the computed edge-distances are at least equal to 4, then nodes with  $C_{k-1}$  will be assigned with  $C_j$  while nodes with  $C_j$  will be assigned with  $C_{k-1}$ .

### Algorithm Two-step Diagnosis

**Input:** Adjacency Graph  $G_{ad}$

- Task1.* Sort the adjacency list  $D \times |V|$   
*Task2.* For  $q = D$  downto 1, select a current uncolored node  $w$  that has the degree of  $q$   
*Task3.* Check all the PSNs of  $w$   
assign the lowest color number to  $w$  as possible  
*Task4.* If there is any uncolored node, then goto *Task2*  
*Task5.* Assign STV to each node  
apply the test and analyze the responds  
if there is no faulty responds, then exit  
*Task6.* Let  $\{F\}$  be a list with nodes that are susceptible to faulty  
foreach faulty node  $u \in V$   
 $\{F\} \leftarrow u$   
find all  $v \in V$  such that  $\{u, v\} \in E$   
 $\{F\} \leftarrow v$   
*Task7.* Remove all edges  $e_{ij}$  from  $G_{ad}$   
iff  $n_i \notin \{F\}$  and  $n_j \notin \{F\}$   
*Task8.* Find the disjoint graph components  $G_{ad}$   
*Task9.* For each  $G_{ads}$ , execute the **One-step Diagnosis Algorithm**

Figure 1. Algorithm for two-step diagnosis.

otherwise,  $j$  is reduced by one and the edge-distance computation procedure is processed again. If there is a successful color swapping, the edge-distance among all the nodes with  $C_k$  and  $C_{k-1}$  will then be at least equal to 4 and node with  $C_k$  can be assigned with color  $C_{k-1}$ . Thus, the number of colors can be reduced by one. The entire procedure is repeated again with the current  $j$  and updated  $k$  until there is no more node with color other than  $C_1$  and  $C_{k-1}$  satisfying the above requirements. The time complexity of Phase 3 is  $O(m \times n^3)$ .

Note that the time complexity of executing Phase 3 appears to be high for a large number of nets under test. But the test generation process is a one-time off-line computation for a specific board or module. Its cost becomes of little concern if the resulted compact test sequence can save the cost in on-line testing. One alternative approach for testing thousands of nets is to execute Phase 1 and Phase 2 only. Test length can be reduced to a reasonable time.

## 4 Two-step Diagnosis

Instead of diagnosing the set of all interconnect faults using the one-step diagnosis algorithm, we have proposed another algorithm for fault diagnosis based on a two-step process. Two-step diagnosis refers to the process that diagnosis is done by applying two test sequences. The results of the first test sequence is used in generating the second test sequence. As the same with one-step diagnosis, the adjacency fault model is assumed. The two-step diagnosis algorithm is shown in Figure 1.

In the first step, test set is generated to detect the presence of faults as well as identifying if each individual net is either fault free or faulty. Besides, both open faults and stuck-at-faults can be detected. Conventional graph coloring is applied to  $G_{ad}$  such that no two adjacent nodes receive the same color. The STV assignment is the same as that in one-step diagnosis. It has been shown that for an arbitrary graph  $G=(V,E)$  with maximum degree  $D$ , the number of colors used is less than or equal to  $(D+1)$  [13]. Thus, the first step yields a low test length as  $D \ll n$  under our adjacency fault model.

With this simple coloring, if there is a short between two adjacent nodes in  $G_{ad}$ , then one of the nodes will receive the fault syndrome as these two nodes are assigned with difference STVs. In other words, if a node receives a syndrome after applying the first test set to the interconnects, then all the edges associated with this

Example	# of net	test length of	test length of	% reduction
		'n+1'	proposed	
		algorithm	approach	
ir232	20	21	16	24%
68hc11	91	92	74	20%
sram8	118	119	92	23%
cperi24	269	270	227	16%

Table 1. Simulation results for benchmark layouts.

Example	test length of	test length of	% reduction
	'n+1'	proposed	
	algorithm	approach	
r100_4	101	56	45%
r200_4	201	118	41%
r500_4	501	277	45%
r1000_4	1001	771	23%
r100_8	101	83	18%
r200_8	201	164	18%
r500_8	501	406	19%
r1000_8	1001	813	19%

Table 2. Simulation results for random interconnects.

node are susceptible to faulty and all the nodes associated with these edges may involve in a short. A fault list is built to store all these nodes. As a result, an edge in  $G_{ad}$  is considered to be fault free only when the two nodes associated with this edge are not in the fault list. The remaining task in the first step is to delete all the fault free edges from  $G_{ad}$  and find (if any) the disjoint graph components of the new  $G_{ad}$ .

In the second step, the one-step algorithm is applied to the resulted graph components for the full diagnosis of interconnect faults. With two-step diagnosis, the test length can be further reduced as  $G_{ad}$  is decomposed into a number of disjoint graph components with reduced number of nodes, especially when the fault rate is low.

## 5 Simulation Results

The proposed one-step diagnosis algorithm was implemented using Cadence SKILL code [15]. The program is tested on a set of real PCB layouts whose adjacency graphs are known. Each board layout contains one power and one ground net, for which no test vectors are needed. The simulation results are shown in Table 1. Note that the power and ground nets are excluded in the test vector generation. The proposed one-step diagnosis approach has also been evaluated by simulation on different size random interconnects with varying maximum degree  $D$ . For example, referring to Table 2, r100\_4 is a randomly generated adjacency graph with 100 nets and  $D$  equal to 4, while r200\_8 contains 200 nets and  $D$  equal to 8. Table 2 shows the simulation results.

For the PCB layouts, the percentage reduction of the test length are less than 30%. One major reason is that their adjacency graphs  $G_{ad}$  are relatively dense with high number of edges and high  $D$ . For randomly generated adjacency graph with  $D=4$ , the test length can be reduced by more than 40%. However, for random  $G_{ad}$  with  $D=8$ , they show a relatively lower percentage reduction. This is due to the fact that in general, adjacency graph constructed with low  $D$  is relatively sparse as compared to that with high  $D$ . Moreover, the execution time is different. As a result, the adjacency fault model has a large impact on the complexity of the proposed approach and the generated test sequence length.

To evaluate the proposed two-step diagnosis algorithm, we

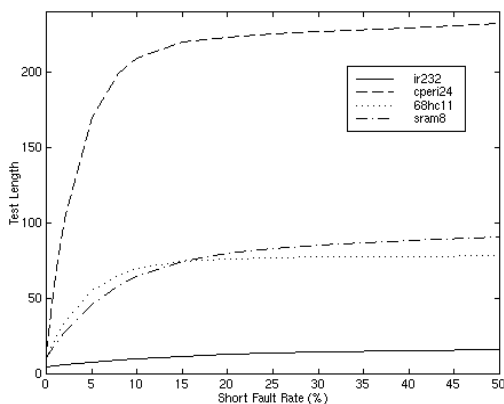


Figure 2. Test length vs. short fault rate in two-step diagnosis for PCB layouts.

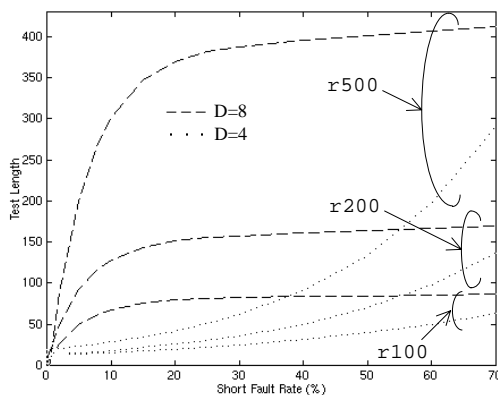


Figure 3. Test length vs. short fault rate in two-step diagnosis for random interconnects.

perform the simulations by randomly injecting faults to the four PCB layouts and random interconnects. The *short fault rate* is defined as the probability of the existence of a short fault for an edge in the adjacency graph  $G_{ad}$ . Figure 2 and Figure 3 show the simulation results for the test length versus short fault rate for the four PCB layouts and the random interconnects respectively. Note that the number of tests for detection required for *ir232*, *68hc11*, *sram8* and *cperi24* in the first step of the two-step diagnosis are 4, 7, 5 and 8 respectively.

The following conclusions can be drawn from the simulation results. The number of tests using the proposed two-step process shows a direct dependency with the short fault rate for diagnosis. With a short fault rate above 20%, it is shown that the test length for all the PCB layouts and the random interconnects with  $D$  equal to 8 are almost equal to that obtained by one-step diagnosis. Thus, two-step diagnosis is not necessary in this case for test length reduction. However, when the short fault rate is very low ( $<5\%$ ), at least a 50% reduction in the test length compared with [12] can be achieved. It can be shown in Figure 3 that random interconnects with different  $D$  exhibit different characteristics. Simulation results show that a 50% reduction in the test length can be achieved with a short fault rate of as high as 60% for random interconnects with  $D=4$ . Again, this is related to the fact that random  $G_{ad}$  with low  $D$  is relatively sparse as compared to that with high  $D$ . As a result, in addition to the short fault rate, the adjacency fault model affects the performance of the two-step diagnosis process.

## 6 Conclusions

This paper has presented a new approach for test vector generation and diagnosis of interconnects for boundary-scan testing. By considering a more complex bridging short fault model in CMOS circuit environment, the test set is generated using graph coloring technique based on the net adjacency relationships in the layout. Our proposed structural approach guarantees the complete diagnosis of multiple interconnect faults and is applicable to both one-step and two-step diagnosis. Simulation results show that the two-step diagnosis approach performs very well when the short fault rate is very small. Besides, for a board in a matured product line, the number of possible primary shorting nets for each net can be reduced under the adjacency fault model. As a result, the test length can be further decreased. This can save the cost for boundary-scan testing.

## Acknowledgment

The authors would like to thank J.T. Sousa at Imperial College, UK, for providing the PCB layout information. This research is supported by Research Grant Council Earmarked Research Grant HKUST 547/94E and Cooperative Research Centre Grant HKUST CRC96/99.EG02.

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