# Estimation of Peak Current through CMOS VLSI Circuit Supply Lines

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*Abstract*— **We present a new approach for estimating the maximum instantaneous current through the power supply lines of CMOS VLSI circuits. Our final goal is to determine the peak currents and voltage drops through power supply lines of real VLSI circuits within a practical time. Our approach is based on the *iMax algorithm*[1] of estimating the upper bound of the current, and uses an improved timed ATPG-based algorithm[2] to obtain a tight lower bound. In order to handle sequential circuits, we equate latch outputs with primary inputs for the upper bound estimation and use a logic simulator to determine the initial values for the lower bound estimation. Based on the information obtained, we model all blocks in the circuit as voltage-controlled current sources, with the analog hardware description language (AHDL). After extracting parasitic resistances of the power supply lines, we simulate the entire circuit using an analog simulator and obtain the maximum current estimation and voltage drops in the supply lines. In the modeling procedure we take the negative feedback influence into consideration such that the estimated current reflects a real switching transition. We have implemented the theoretically modeled negative feedback influence into our simulator called PANGI. Some experimental results of applying PANGI to the circuits which consist of more than 1M gates prove the accuracy and reliability of our approach.**

## I. Introduction

As the number of gates fabricated on a chip grows higher, simultaneous switching current through the power supply lines becomes larger. Excessive current may severely affect both the circuit reliability and performance due to excessive voltage drops and bounces in the supply lines. These voltage fluctuations cause erroneous logic signals (false switching) and degradation of the switching speed.

In this paper, we report the results of our approach for estimating the peak currents and voltage drops through power supply lines of CMOS VLSI circuits. We propose an improved timed ATPG-based algorithm which determines a tighter lower bound of the peak current. Based on such information, we refine the estimated values by simulation using an analog simulator and consideration of the negative feedback influence. Experimental results confirm that our approach can lead to an accurate estimation within a practical time.

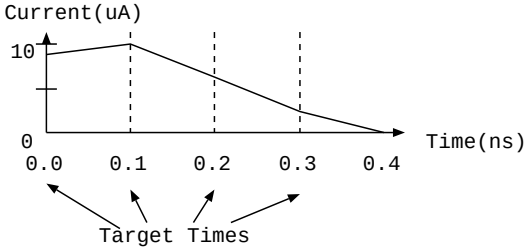


Fig. 1. Maximum Envelope Current and Target Times

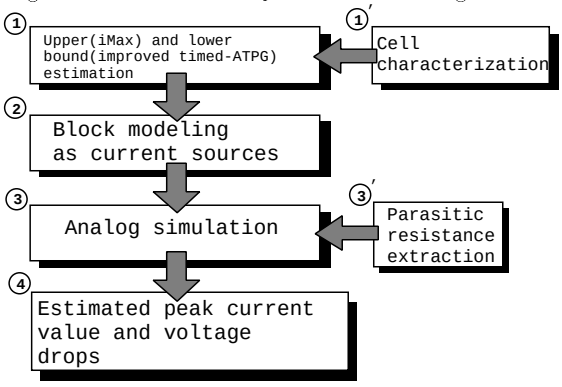


Fig. 2. Estimation Process

The remainder of this paper is organized as follows. Section II briefly introduces the previous work. Section III describes our process of estimating the peak current and voltage drops. In section IV, we explain an improved timed ATPG algorithm adopted in our approach. In section V, we discuss how to extend the algorithm to handle sequential circuits. In section VI the theoretical negative feedback influence model is introduced. Section VII shows some experimental results, and concluding remarks are given in section VIII.

## II. Previous Work

Power supply currents depend on the specific input patterns applied to the logic circuit. Since it is prohibitively expensive to simulate all possible input patterns using a conventional dynamic simulator, many static approaches have been proposed. The *iMax algorithm*[1] is a powerful

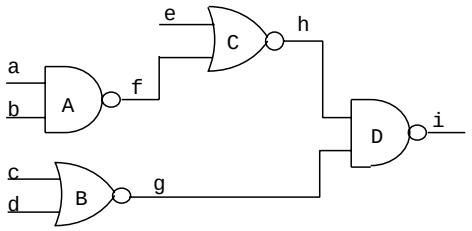


Fig. 3. Example Circuit

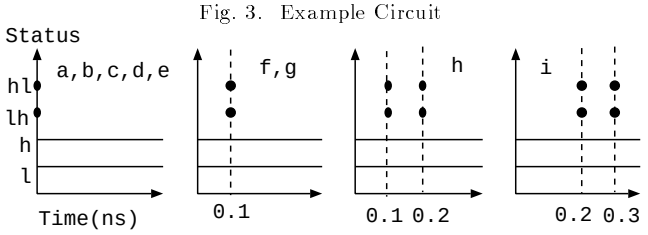


Fig. 4. Uncertain Waveform of iMax Algorithm

method of estimating the upper bound of the current statistically. A timed ATPG-based algorithm starting from the *iMax* result was presented to obtain a lower bound of the current[2]. Since this algorithm gives priority to speed over finding an optimal solution, it gives a somewhat loose lower bound.

*iMax* assumes that all inputs to the combinational logic switch simultaneously at time t=0 for CMOS circuits with an arbitrary delay. It also assumes that the switching current has a right-angled triangular form. The peak current is assumed to occur at the input transition. In *iMax*, at any point of time, a signal is assumed to have one out of four possible excitations: stable 1 value (h), stable 0 value (l), rising transition (lh) or falling transition (hl).

*Uncertainty waveforms*[1] represent all possible excitations that a signal can have over any input pattern applied to the primary inputs. Using this uncertainty waveform, we can obtain the *Maximum Envelope Current (MEC)* waveform which represents the upper bound of the current (Fig.1).

For the lower bound, a timed ATPG-based algorithm [2] selects several "target times" and determines the possible primary inputs that maximize the current at that target time. Our approach leads to some improvements in these *iMax* and timed ATPG-based algorithms.

## III. Estimation Process

Our approach is illustrated in Fig.2. It is based on the *iMax algorithm* in the first step of determining the upper bound. First, using the *iMax algorithm* and the improved timed ATPG algorithm, we estimate a peak current. Here, in order to obtain accurate peak current values and the switching duration time, we consult the lookup tables for delay and switching current values for each gate, which have been characterized and prepared beforehand for a conventional logic simulation (Fig.2-①').

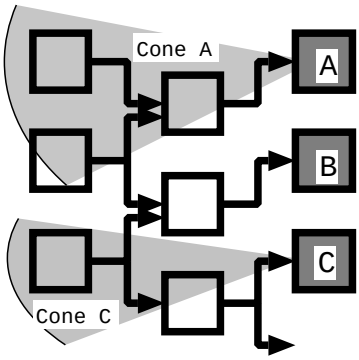


Fig. 5. Input Path Cones

According to the calculated peak currents, all blocks are modeled as voltage-controlled current sources. These current sources are modeled so as to take into consideration the negative feedback influence using the AHDL (Fig.2-②).

Finally, we invoke an analog simulator (Fig.2-③) for the netlist containing the parasitic resistances of the supply lines (Fig.2-③') and obtain the voltage drops and improved current values (Fig.2-③).

## IV. Static Lower Bound Estimation

In this section, we focus on combinational blocks of edge-triggered latch-controlled synchronous digital circuits. In section V, we discuss one of the approaches for including the other sequential blocks.

### A. Algorithm

Our aim is to find a set of two-vector patterns which would produce a maximal switching current. Using the *iMax algorithm*, we can obtain the current waveform of the upper bound. Starting from this current waveform, our algorithm tries to determine a tight lower bound by finding independent input paths to active gates. By avoiding collision of the justification path of the active gates as much as possible, we obtain a tight lower bound of the current. Our algorithm is as follows.

- Step 1. We determine the target time which has the largest current value in the target time list which initially contains all target times, and then determine the active gates at that time. These active gates are sorted according to the amount of contribution of each gate to the current.
- Step 2. An input path cone (Fig. 5) for each active gate is created. The cone is a set of nodes which affects the behavior of the gate. Starting from the gate with the greatest contribution, we first assign the required transition to it. Using the information about the target time $T$ and gate delays, we search the path from the gate to the primary input in the cone which lead to the transition. In this process, we first try to find a path not included in other cones. If the absence of such a path, the path whose current contribution to the other gates is the smallest is searched. In the case of a conflict in this phase, we backtrack and find another path. If nonetheless, the conflict cannot be resolved, we choose the gate whose longest path is longer than the other and resensitize the path. If the current gate has only shorter paths,the transition of the gate is changed.
- Step 3. After all gates in the target set have been processed, we check if the justification list is empty.

- Step 4. We quit if the estimated lower bound of the current is greater than the upper bound at the next target time determined by the *iMax algorithm*. If not, the target time in the target time list is deleted and we go back to Step 1.

### B. Example

Consider the circuit shown in Fig. 3. Using this circuit, we obtain the uncertainty waveform shown in Fig. 4. For simplicity, we assume that the gate delays and current contributions of all gates are the same.

1. From the uncertainty waveform information, the target times are listed as {0.1ns, 0.0ns, 0.2ns, 0.3ns} in ordered of their current contributions.
2. First, we select 0.1ns as a target time, since its current contribution is the highest. At that time, active gates are listed as {A, B, C, D}. Then, for each gate, an input path cone is created. For example, the input path cone for gate D is the set of nodes {a, b, e, f, h}. Gates C and D contribute most to the current at that time. In a case like this where values are equal, we choose the gate whose input path cone has many independent paths, i.e., paths which do not belong to other gate cones. In this case, we select gate D and the path e→h→D. Since the rising and falling transitions transmit the same amount of current, we randomly assign a falling transition to node i, a rising transition to node h and a falling transition to node e. Similarly, we sensitize the path a→f→C and the path c→g→D. Next we pick gate C and select the path b→f→C and assign a rising transition to it. Here there is no conflict. Processing all gates in this manner, we obtain the following primary input justifications.

| node | transition |
|---|---|
| a, b | rising |
| c, d, e | falling |

3. Now, all gates are justified and all primary inputs are determined.
4. 0.1ns is deleted from the target time list and we go back to Step 1.

## V. Extension to Sequential Circuits

In order to be applied to industrial circuits, sequential blocks should be handled properly. In this section, we consider the extension of the above approach to sequential circuits.

We can easily obtain the upper bound of the current by treating the outputs of the flip-flops and latches as primary inputs, since we can assume that all the gates switch simultaneously in synchrony with the clock. On the other hand, the lower bound estimation is rather difficult. We use the node states immediately after a reset signal is applied to the circuit as initial states of flip-flops and constrain the justification process to these transitions. In order to obtain these after-reset values, we invoke a logic simulator and an input vector created by the circuit designer. This approach has the drawback that the designer is expected to create a suitable input vector for current estimation and the accuracy largely depends upon the quality of the input vector. Our current implementation adopt these algorithms and thus should be studied further.

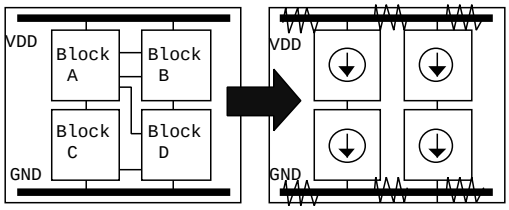


Fig. 6. Block Model with Negative Feedback Influence and Chip-level Model

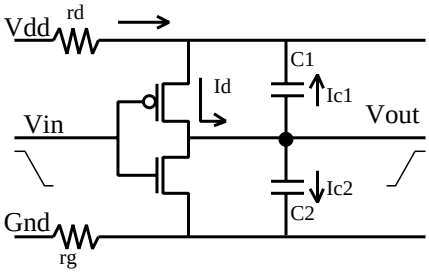


Fig. 7. Model of Negative Feedback Influence

## VI. Model of Negative Feedback Influence

Up to now, we have assumed that the supply lines remain at the same voltage. However, due to the parasitic resistance of the supply lines, excessive current causes severe voltage drops in power and ground buses [3]. Since voltage drops reduce the switching current, we must model their influence to reflect the actual switching behavior.

According to Sakurai and Newton[4], the drain current $I_D$ is approximated as

$$I_d = \begin{cases} 0 & (V_{GS} \le V_{th} : Cut-off\ region) \\ K(V_{GS}-V_{th})^{\frac{\alpha}{2}} V_{DS} & \\ & (V'_{DS} < V_{D0} : linear\ region) \\ K(V_{GS}-V_{th})^{\alpha} & \\ & (V_{DS} \ge V'_{D0} : saturation\ region), \end{cases}$$

where $K$ is a drivability factor and equals $\mu \frac{\epsilon_{ox}}{t_{ox}} \frac{W}{L_{eff}}$ where $\mu$ denotes the effective mobility, $\epsilon_{ox}$ the dielectric constant of the gate oxide, $t_{ox}$ a gate oxide thickness, $W$ the channel width, and $L_{eff}$ the effective channel length.

In deep-submicron CMOS circuits, all switching transistors remain in the saturation region during the switching transition due to the velocity saturation effect [5]. Additionally, the smaller the gate length becomes, the closer the $\alpha$ moves to 1. Consequently we can assume that $\alpha$ is equal to 1 without loss of accuracy.

As shown in Fig. 7, the following relationships are formulated.

$$\begin{cases} I_d &= K\{V_{dd} - V_{th} - (I_d - I_{C1})r_d - (1 - \frac{t}{t_{sr}})V_{dd}\} \\ I_{C1} &= C_1 \frac{d[V_{out} - \{V_{dd} - V_{th} - (I_d - I_{C1})r_d\}]}{dt} \\ &= \frac{C_1}{C_1 + C_2} I_d \\ & (t \ge t_{sr}\frac{V_{th}}{V_{dd}}). \end{cases}$$

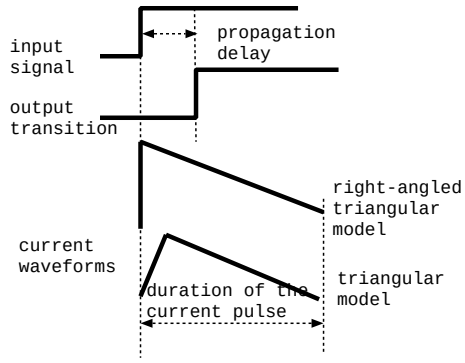


Fig. 8. Model of Current Waveform

Here, $t_{sr}$ is the transition time of the input signal (slew rate). From these equations, we obtain

$$\begin{cases} I_d &= \dfrac{K(tVdd - t_{sr}V_{th})}{\{C_1 + C_2(1+Kr_d)\}t_{sr}} \\ V_{out} &= \dfrac{KV_{dd}}{2\{C_1 + C_2(1+Kr_d)\}t_{sr}}t^2 \\ & \quad -\dfrac{V_{th}t_{sr} - KC_2V_{dd}r_d}{\{C_1 + C_2(1+Kr_d)\}t_{sr}}t + C \\ & \quad (t \geq t_{sr}\frac{V_{th}}{V_{dd}}), \end{cases}$$

where $C$ is a constant such that $V_{out} = 0$ when $t = t_{sr}\frac{V_{th}}{V_{dd}}$. Since in CMOS, whenever a gate undergoes a transition, it can be reduced to an equivalent inverter, we adopt a triangular model as a transition current waveform model of any gate instead of a right-angled triangular model (Fig. 8).

## VII. Experimental Results

### A. Accuracy and performance

We have applied PANGI to several industrial circuits in which the number of gates ranges from 100 to 2Meg. CPU times for those simulations are as follows.

| circuit | # of gates | CPU time (day) (SUN ULTRA 60 300MHz) |
|---|---|---|
| Circuit A (Memory Circuit) | 80,000 | 0.5 |
| Circuit B (Graphics Circuit) | 2,000,000 | 2.5 |
| Circuit C (Graphics Circuit) | 2,000,000 | 2.5 |

It is difficult to compare the accuracies of the estimated values and the actual results. However, several fundamental experiments confirm that our approach is very accurate. In the process of creating lookup tables (Fig.2-①'), the error is guaranteed to be within 10 to 15 %. The error induced by the upper and lower bound estimation is considered about 10%. In many cases, the total error is less than 20% compared to a conventional analog simulation.

### B. False switching detection

In step ③ in Fig.2, PANGI simulates the entire circuit with blocks modeled as the current sources and parasitic resistances of the supply lines. During this process, voltage drops of the supply lines are calculated (Fig. 6). Using the voltage drop results, PANGI determines the possibility of a false switching considering logic connections.

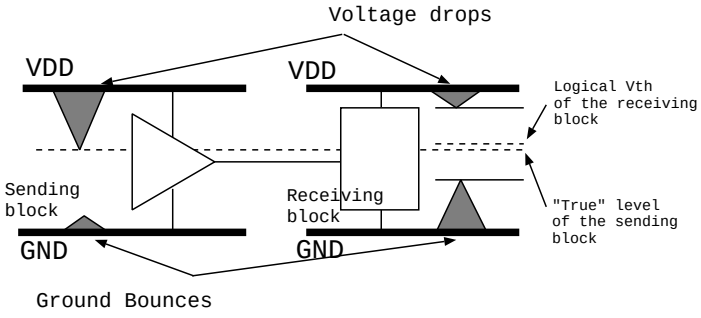


Fig. 9. Fault Switching Simulation Result

As shown in Fig. 9, voltage drops in a sending block can cause a fanout block to receive a wrong signal even though the output remains in the same state, since the logical $Vth$ of the receiving end becomes higher than the "true" level of the sending buffer. PANGI warns of such a possibility by comparing voltage drops of sending and receiving ends and logical $Vth's$ taking into consideration the logic connection information.

In circuit A, PANGI issued a warning of false switching which was verified through the measurement of the real chip.

## VIII. Conclusions and Future Work

We have shown that our approach can be used to estimate the peak current and voltage drops in CMOS VLSI circuits. In the estimation process, we utilized the *iMax algorithm* and also indicated that sequential circuits are also handled via simple extensions to the algorithm. Experimental results for industrial circuits indicated that the algorithm can be a reliable design guideline for the designers of circuits for practical uses.

As of now, a tight lower bound for sequential circuits has not been obtained. The future direction of our study is to find a reliable and fast method of obtaining a tight lower bound for sequential circuits.

## Acknowledgments

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