A Single-Chip CMOS CCD Camera Interface Circuit with Digitally Controlled AGC

Jin-Kug Lee*, Dong-Young Chang**, Geun-Soon Kang**, and Seung-Hoon Lee*

* Dept. of Electronics Engineering, Sogang University, Seoul, Korea
** Samsung Electronics Co., Ltd., Yongin, Korea

TEL: +82-2-705-8471, FAX: +82-2-706-216, e-mail: hoonlee@ccs.sogang.ac.kr

Abstract—This paper describes a single-chip solution for CMOS CCD camera interface systems. The required AGC gain in the proposed circuit is controlled directly by digital bits without conventional extra DAC's. Nonlinear errors such as offsets in signal paths are automatically removed during black-level correction. The AGC outputs are transferred to a 10b on-chip ADC. The prototype implemented in a 0.5um n-well CMOS process shows the 32-dB AGC dynamic range in 1/8-dB step with 173 mW at 3 V and 25 MHz.

I. INTRODUCTION

Recently, Digital Signal Processing (DSP) has been one of major techniques for Charge-Coupled Devices (CCD) applications such as scanners, portable camcorders, and digital still cameras. The trend has increased needs for interface circuits which convert CCD image to digital data [1]. Considering that the CCD image information is composed of a series of 'reference' and 'data' levels, the interface circuits need to carry out three essential roles: Correlated Double Sampling (CDS) which means a sampling of the difference between the 'reference' and 'data' signals from the CCD with eliminated 1/f noise, Automatic Gain Control (AGC) which controls a required gain of the output signal from the CDS, and A/D Conversion which transforms the analog signal from the AGC into a digital word.

Most of the conventional CDS and AGC circuits have been implemented in bipolar or BICMOS technologies and separated from standalone CMOS A/D Converters (ADCs). It increased engineering costs and clock skew problems between distinct chips. Recent single-chip CMOS systems merged the multiple interface functions in a single chip and demonstrated a reduced cost and an increased performance [2]-[4]. However, some interface systems are based on more than three Sample-and-Hold Amplifiers (SHAs) for the CDS circuit at the expense of power and chip area. The other systems employ only two SHAs for the same CDS function, but still need to adjust the system timing to be compatible with the circuit blocks such as the back-end ADC [3]-[4]. On the other hand, the conventional AGC circuits typically have required extra D/A Converters (DACs) to control the gain in the analog domain corresponding to the external digital gain control bits (GCIBs) [5]-[6].

This work focuses on the following five design techniques based on a CMOS technology. First, fully differential structures are employed throughout the chip to minimize noise pickup and to obtain a wide signal swing on a 3V to 5V supply voltage. Second, the CDS composed of only two SHAs takes image information out of the CCD with the identical two-phase non-overlapping clock used in the ADC. Third, the proposed digitally controlled AGC amplifies signals over a wide range in a fine step of a 1/8-dB level and a gain-independent settling time is achieved by adjusting the sampling capacitor size. Fourth, a power reduction technique is applied to analog circuit blocks to reduce total power dissipation [7]. Last, nonlinear errors such as offsets and feedthrough in the front-end signal loop are measured and stored by the on-chip integrator during periodic black-level correction and automatically eliminated during normal conversion process.

II. PROPOSED FRONT-END CIRCUIT

A. System Architecture

The front-end circuit samples the voltage difference between the 'reference' and 'data' signals to send the CCD image information to the back-end ADC accurately, while adjusting the black level of the sampled signal to the lowest reference level of the ADC. As shown in Fig. 1, the proposed interface circuit consists of four blocks: CDS, AGC, Loop Gain Control (LGC), and INTEGRATOR (INT). The single-ended image signal from the CCD image sensor is sampled and converted to the fully differential signal by the CDS for the remaining circuit blocks. The CDS subtracts the INT output from the sampled image signal. The AGC samples and amplifies the difference between two differential signals from the CDS, based on the GCIBs from the external DSP. The amplified AGC output is transferred to the input SHA of the back-end ADC.

During periodic black-level correction, the CCD image sensor sends the optical black-level signal from metal-covered pixels to the 'data' of the CDS, to match the CCD black level and the ADC
reference bottom. At this time, the feedback loop through the LGC and the INT is activated. The LGC compares the black-level signal amplified by the AGC with the ADC reference bottom voltage and transmits the difference to the INT. The INT accumulates the LGC output for the CDS. The CDS subtracts the INT output from the sampled black-level signal and passes the difference to the AGC. In this way, the black-level signal is matched to the lowest reference voltage of the ADC. On the other hand, the nonlinear errors such as feedthrough, offsets, and a minor gain mismatch in the feedback loop appear as an input offset voltage of the ADC. In the proposed system, the undesired errors are automatically sampled and stored in the INT during the black-level correction period.

While image signals from the CCD are being sent to the CDS during normal data processing, the feedback loop is turned off with the LGC deactivated. When the magnitude of the CCD signal is much smaller (or larger) than the full-scale voltage of the ADC, the signal needs to be increased (or decreased) by the AGC. The external DSP analyzes the ADC outputs and generates 8b digital control signal to adjust the AGC gain. The AGC gain and the nonlinear errors in the signal paths are optimized so that the ADC can always use the full-scale input dynamic range matched to the reference.

B. CDS Circuit

The CDS samples the voltage difference between the 'reference' and 'data' signals from the CCD and removes correlated nonlinear errors such as reset noise and 1/f noise in input signals [8].

The proposed CDS, as illustrated in Fig. 2, is composed of two SHAs and operated by two non-overlapping clock phases for the back-end ADC without any system timing modification. The CDS operates as follows. At Q1, switches S1, S2, and S6, are closed so that the SHA1 can sample the voltage difference between the 'reference' and the INT output. At Q2, switches S1, S2, and S6, are open while switches S3, S4, and S5, are closed. The SHA1 transfers the sampled differential signal to the AGC and the SHA2 samples the difference between 'data' and the INT output. At the next Q1 phase, the SHA2 output is connected to the AGC. Simultaneously, the AGC amplifies the difference between the SHA1 output sampled at the former Q1 and the SHA2 output sampled at the former Q2. As results, the CDS obtains the required voltage difference of the CCD video signals, 'reference' and 'data', with the reference to the INT output stored during black-level correction.

C. AGC and LGC Circuits

The AGC amplifies the CDS analog output by required gains. The AGC gains can be typically decided by analog voltages or external digital GCBs. In most of analog voltage-controlled AGC circuits, the open loop gain of amplifiers is varied by the analog control voltage and an extra DAC is required to produce the control voltage from the external GCBs. The DAC increases system costs, power consumption, and die area. On the other hand, conventional digitally-controlled AGC circuits are operated by changing the size of the feedback and sampling capacitors according to the GCBs. In the AGC circuits, the feedback gains change due to variations of the ratio between the feedback and sampling capacitors. The resultant frequency response and settling time are difficult to be optimized and the operation speed is limited by the slowest capacitor combination. Moreover, the architecture employing an array of binary-weighted capacitors makes a fine gain control extremely difficult [9]-[10].

The proposed AGC function is achieved by interchanging the sampling capacitors corresponding to the GCBs. A sampling capacitor array weighted by a required fine gain step, \(a\), along with a unit feedback capacitor, \(C\), is implemented in Figs. 3(a) and 3(b). The gain \(a\) is obtained from the op amp output by the ratio between the sampling capacitor, \(aC\), selected by the GCBs and the unit feedback capacitor, \(C\), during amplification, which removes the necessity of extra DACs. On the other hand, since the feedback gain in the amplifying phase is fixed by keeping the total sampling capacitance constant, the op amp bandwidth is independent of gain variations and a
constant settling time of the AGC is obtained. In addition, a fine gain control is achievable by minimizing the gain step, $a^0$, within process limitation.

When the required resolution of the GCBs is increased, the number of the total sampling capacitors grows exponentially and degrades the frequency response of the AGC seriously. The proposed AGC overcomes the limitation by dividing the single amplifying function into three stages. The first stage that samples the difference between two differential signals from two SHAs in the CDS, is controlled by the MSB of the GCBs for simplicity. The gain step of this stage is set to 16 dB corresponding to the MSB. The gains of the second and third stages are controlled by three LSBs and four middle bits, with the gain steps of 1/8 dB and 1 dB, respectively. Four middle GCBs in the third stage make the total sampling capacitance the largest out of the three stages, which prevents the op amp from high speed operation. The proposed capacitor combination technique in the third stage minimizes the total sampling capacitance and the feedback gain of the op amp. The larger sampling capacitors for higher gains are realized by the parallel combination of small capacitors used for lower gains. The combination is obtained by the capacitor combination logic with the four middle GCBs, as shown in Fig. 4. For example, with 0000 of the GCBs, the sampling capacitor $C$ is connected to the 'VIn' and the others to GND, which results in the gain of $a^0$. With 0001, $C$ and $C_1$ are connected to 'VIn', for the gain of $a^1$. The size of $C_1$ is determined from $[C + C_1 = a^1 C]$. The sizes of the remaining capacitors, $C_2, ..., C_{15}$, are calculated in the same way. When the maximum gain is requested, all capacitors, $C, C_1, ..., C_{15}$, are connected to 'VIn' for a $a^{15}$. By applying the technique, the total sampling capacitance is reduced from 44C to 6C, in 1-dB gain step, approximately. As results, the minimized feedback gain and the high speed operation of the op amp in the third stage are obtained simultaneously.

The LGC in the feedback loop maintains the loop gain of the front-end circuit constant during black-level correction. The sampling capacitors are arranged in the reverse order of the suggested AGC and the feedback capacitor size is set to the largest sampling capacitance. The LGC attenuates the signals as much as the AGC amplifies.

III. BACK-END ON-CHIP ADC

The back-end 10b 25MHz four-step pipelined ADC integrated on the same chip is shown in Fig. 5. The ADC consists of an SHA, three Multiplying D/A converters (MDACs), four flash ADCs, and digital correction logic (DCL). The first stage decides four bits, while the remaining stages decide three bits to improve yield by minimizing input-referred component mismatch effects[11]. A power reduction technique employed on the analog circuit blocks such as the residue amplifiers of the MDACs reduces the ADC power dissipation without degrading the basic function at a high speed [7].

IV. EXPERIMENTAL RESULTS

The proposed CCD camera interface circuit was implemented in a 0.5 μm double-poly double-metal n-well CMOS process. The measured characteristic of the AGC with the 32-dB dynamic range in 1/8-dB step is plotted in Fig. 6.

As shown in Fig. 7, the DNL and INL of the back-end ADC are within ±0.7 LSB. The measured SNDR versus sampling frequency are plotted in Fig. 8 where the input frequency is kept constant at 1 MHz. A die photo of the prototype in Fig. 9 occupies the active area of 2.2 mm ×
4.0 mm and an image picture captured by the prototype and a commercial digital camcorder with a 9.6 MHz sampling frequency and a 12-dB gain is illustrated in Fig. 10. The typical performance of the proposed single-chip CCD interface system is summarized in Table I.

![Diagram of ADC block diagram](image)

**Fig. 5. ADC block diagram.**

![Graph of AGC gain control code](image)

**Fig. 6. AGC characteristic.**

![Graph of DNL and INL plots of the ADC](image)

**Fig. 7. DNL and INL plots of the ADC.**

![Graph of SNDR versus sampling frequency](image)

**Fig. 8. SNDR versus sampling frequency (f_s=1 MHz).**

**Fig. 9. Chip photograph (2.2 mm × 4.0 mm).**

![Graph of typical performance of the proposed CCD interface circuit](image)

**Fig. 10. Picture captured by the prototype.**

**TABLE I. Typical Performance of the Proposed CCD Interface Circuit.**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Speed</td>
<td>25 MHz</td>
</tr>
<tr>
<td>Power</td>
<td>173 mW (at 3 V)</td>
</tr>
<tr>
<td></td>
<td>346 mW (at 5 V)</td>
</tr>
<tr>
<td>AGC Dynamic Range</td>
<td>0 ~ 32 dB (1/8 dB step)</td>
</tr>
<tr>
<td>Supply Voltage</td>
<td>3 V ~ 5 V</td>
</tr>
</tbody>
</table>

**REFERENCES**


