Electronics Development of Silicon Microdisplay for Virtual Reality Applications

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Abstract - We have developed a highly integrated liquid-crystal-on-silicon microdisplay for virtual reality applications. The silicon display panel was designed and fabricated by a custom 0.5μm 3-metal CMOS technology. We further utilized field programmable gate array to implement a color sequential technique for driving this display panel. 4 bits per color of the display was demonstrated. The use of FPGA has advantages of fast prototyping and flexible in-circuit reconfiguration for different display applications. This compact microdisplay system can lead to a variety of virtual reality applications.

I. Introduction

Crystalline silicon has been well recognized as an alternative approach for the fabrication of active matrix liquid crystal display (AMLCD)[1]. The advantages are better electronic properties and more matured silicon fabrication technology. Very sophisticated driver circuitry and very fine pixel can be integrated together as a self-contained high-resolution display. Monolithic integration of drivers into the display also helps simplify interconnection and packaging problems associated with the display system. As a result, the silicon microdisplay is very suitable for virtual reality (VR) applications where small physical size and low power consumption are decided advantages. Traditional virtual reality displays based on cathode ray tube (CRT), light emitting diode (LED) or thin-film transistor liquid crystal display (TFT-LCD) are either too bulky or very power consumptive[2,3,4]. In this work, we present electronics development of silicon microdisplay particularly for virtual reality applications.

II. Silicon Microdisplay Panel

Figure 1 shows functional block diagram of the silicon microdisplay panel. Only two control signals are required. Whereas, FLM marks the first line and DISP points to the first pixel of each line. The 4-bit pixel data are shifted in series to data drivers and transferred in parallel to D/A converters where the D/A conversions are performed. External reference voltages for the D/A converters are to tailor very nonlinear reflectance-vs-voltage curves of liquid crystal with respect to different color illumination. With integrated high-speed digital data drivers, the pixel clock can go up to 100MHz which corresponds to 10ns pixel access time. The display panel has 400x300 pixels, or 1/4 SVGA resolution. The pixel pitch is 25μm and fill as factor is 91% as a result of 0.5μm layout rules. Figure 2 shows photograph of one corner of the silicon display panel. Data drivers on the top, scan drivers on the left are visible together with the pixel array in the centre.

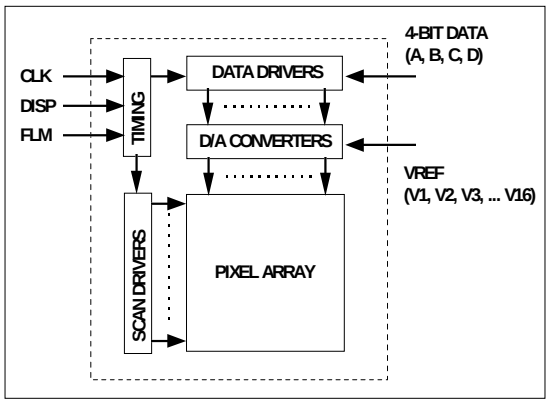

Figure 1. Functional block diagram of the silicon microdisplay panel.

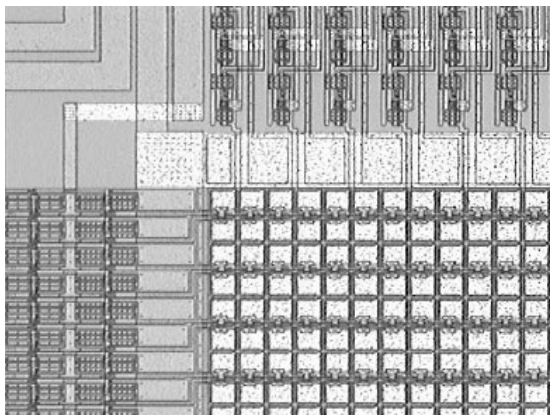

Figure 2. Photograph of one corner of the silicon microdisplay panel.

III. Liquid Crystal on Silicon

Figure 3 shows cross section of the liquid-crystal-on-silicon structure. Pixel transistor acts as a sample-and-hold device where gate and drain of the transistor are connected to scan and data drivers, respectively. The surface of pixel metals is planarized by chemical-mechanical polishing for an optical-grade flatness. A black matrix is inserted beneath the pixel metals for light shield. The glass plate is coated with a layer of indium tin oxide (ITO) which acts as a transparent electrode. Liquid crystal is filled into the gap between the silicon substrate and glass plate where the cell gap is controlled by spacers for required retardation.

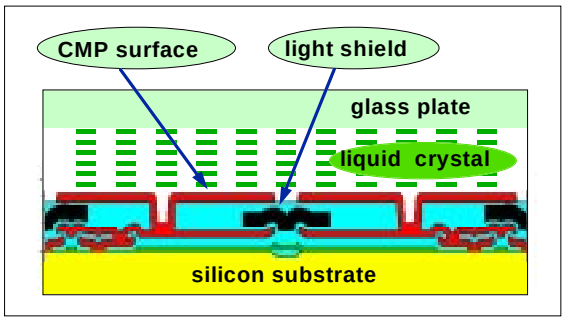

Figure 3. Cross section of the liquid-crystal-on-silicon structure.

Figure 4 shows reflectance-vs-voltage curves of the liquid crystal (LC) cell for three primary colors as characterized by a 3-color-in-1 LED. The contrast ratios were 49, 32 and 21, respectively under red, green and blue light illumination at 3 Vrms. Whereas, bright state occurred at 1 Vrms and dark state occurred at 3 Vrms. With polynomial curve fitting of the reflectance-vs-voltage curves as shown in Figure 4, we proceeded to obtain gamma-correction resistor network to provide 16 true gray-scale LC driving voltages. This gamma-correction resistor network is deemed required in order to implement a color sequential display of true color.

IV. Smart Display System

Figure 5 shows block diagram of the smart display system. The smart display system is an application specific circuit for driving the silicon microdisplay for different display applications. As shown in Figure 5, the smart display system can accept digital video signal such as MPEG, or analog video signal such as NTSC or PAL.

For analog video input, the display system firstly extracts video data and synchronization signals by a video signal decoder. The synchronization signals are used to generate pixel clock through a phase-locked-loop (PLL) frequency synthesizer. The analog video data are amplified by video amplifiers and converted to 4-bit digital data per color through flash A/D converters. For digital video input, both digital video data and pixel clock are available. Hence, the pixel clock extraction and video data digitization are not required.

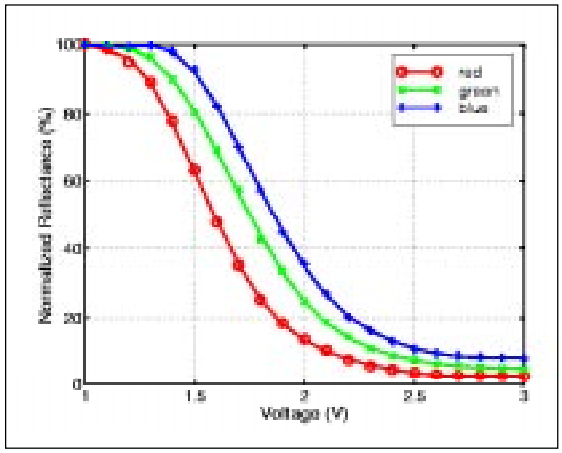

Figure 4. Reflectance-vs-voltage curves of the LC cell for three primary colors.

The heart of the smart display system is the logic control application specific integrated circuit (ASIC) implemented by Xilinx field programmable gate array (FPGA). The logic control ASIC is responsible for video data manipulation and display timing synchronization. It requires different configurations for different display applications. The use of FPGA as the logic control ASIC has advantages of fast prototyping and flexible in-circuit reconfigurations for different display applications.

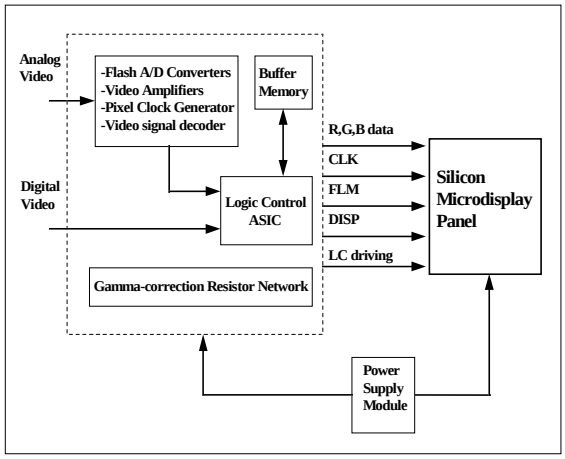

Figure 5. Block diagram of the smart display system.

V. Color-Sequential Technique

We used the logic control ASIC to implement a color sequential technique for driving the silicon microdisplay. Figure 6 shows a schematic of the color sequential technique applied to the silicon microdisplay[5]. The parallel red (R), green (G) and blue (B) video signals are firstly stored in a buffer memory. Thereafter, R, G and B signals are written into the microdisplay in sequence. There are three phases in each R, G or B sub-frame. The first phase is data loading phase in which the corresponding R, G or B sub-frame is loaded. The pixel access time and display resolution determine the period of this phase. With 10ns pixel access time provided by the high bandwidth digital data driver, it takes exactly 1.2ms to load each sub-frame for the microdisplay of 400x300 pixels. The second phase is liquid crystal response phase in which the liquid crystal responds to each loaded sub-frame. The liquid crystal response time, especially the falling time which is usually longer than the rising one, determines the minimum length of this phase. The response time of our mixed-mode twisted nematic (MTN) liquid crystal cell was 18ms[6], whereas the rising time was 6ms and the falling time was 12ms. Hence, a minimum 12ms liquid crystal response phase is required for this MTN cell to be fully responded. The third phase is LED illumination phase in which corresponding R, G or B LED is turned on and illuminates on the microdisplay. LED radiance intensity and system luminance requirement determine the minimum pulse width of this phase. In the experiment, a 2ms pulse could provide enough luminance for our display with an ultra bright 3-color-in-1 LED.

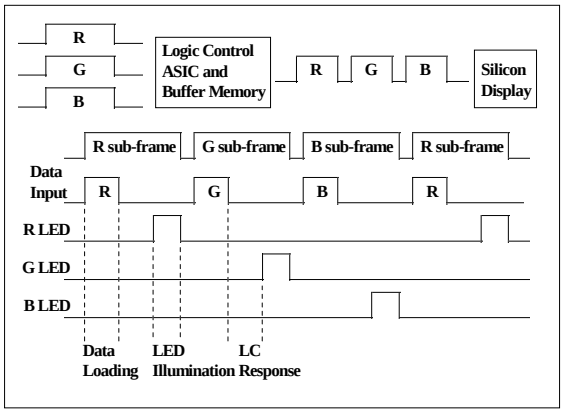

Figure 6. Schematic of the color sequential technique applied to the silicon microdisplay.

Figure 7 shows the logic control ASIC interfaced with the microdisplay panel and buffer memory for color-sequential display. Two memory banks were used to store the R, G and B video data for reading and writing, respectively. While memory bank A was reading 12-bit R, G and B video data in parallel, memory bank B was writing R, G and B video data in sequence to the microdisplay shown in Figure 7. The video data reading clock was synchronized with the input video data at 25MHz. The video data writing clock was increased to 50MHz in order to write the whole frame of video data into the microdisplay within the 180Hz subframe time.

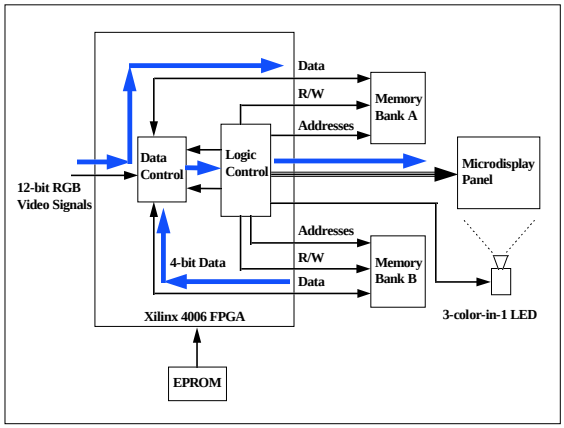

Figure 7. Functional block diagram of the color sequential display system.

Color illumination and display control signals were all generated by the logic control ASIC in synchronization. We used Xilinx 4006 FPGA to implement this logic control ASIC. The equivalent gate count was 5000 and 95 I/O pins were used. The configuration data of the Xilinx FPGA were stored in EPROM. In-circuit reconfiguration of the Xilinx FPGA for MPEG-1, NTSC, PAL and 1/4 SVGA display formats was possible.

Figure 8 shows color viewgraphs of the silicon microdisplay interfaced with personal computer. Vivid images of 4096 colors were demonstrated at 1/4 SVGA display format.

VI. Conclusion

In summary, we have developed a highly integrated silicon microdisplay using a custom 0.5μm CMOS technology. We have also developed a smart display system using FPGA as logic control ASIC for video data manipulation, display timing control and flexible in-circuit reconfiguration. Color sequential technique was used for driving this microdisplay and vivid images of 4096 color was

demonstrated. We believe that this compact microdisplay system can lead to a variety of virtual reality applications with simple head-mounted display optics.

Figure 8. Color viewgraphs of the microdisplay.

VII. Acknowledgment

This work was partially supported by Industry Department of the Government of the Hong Kong Special Administration Region.

VIII. References

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