

# An Automatic Router for the Pin Grid Array Package\*

Shuenn-Shi Chen<sup>1</sup>, Jong-Jang Chen<sup>1</sup>, Sao-Jie Chen<sup>1</sup>, and Chia-Chun Tsai<sup>2</sup>

<sup>1</sup>Department of Electrical Engineering  
National Taiwan University  
Taipei, Taiwan, Republic of China

<sup>2</sup>Department of Electronic Engineering  
National Taipei University of Technology  
Taipei, Taiwan, Republic of China

## Abstract

A Pin-Grid-Array (PGA) package router is presented in this paper. Given a chip cavity with a number of I/O pads around its boundary and an equivalent number of pins distributed on the substrate, the objective of the router is to complete the planar interconnection of pad-to-pin nets on one or more layers. This router consists of three phases: layer assignment, topological routing, and geometrical routing. Examples tested on a windows-based environment show that our router is efficient and can complete the routing task with less substrate layers. Compared to the manual routing, this router owns a friendly graphic user interface and can be practically applied to VLSI packaging.

## 1. Introduction

Nowadays, the electronics industry has grown tremendously. The success was attributed to the revolutionary technology breakthrough in the fabrication process and electronic packaging of integrated circuits. Especially, Pin-Grid-Array (PGA) and Ball-Grid-Array (BGA) packages are complex structures with large peripheral I/O counts, multiple routing layers and built-in decoupling capacitors. As a result, developing an industrial-strength CAD tool for package design becomes indispensable. In past years, many studies on high-speed transmission, power dissipation, noise, and crosstalk for package layout, have been presented [1-3].

A typical PGA package structure containing a chip cavity with a number of peripheral I/O pads and a rectangular array of pins was reported by Lewis [4]. Based on this package structure [4], Tsai and Chen proposed a slope method and a rubber-band like method for the PGA package routing, respectively in [5] and [6]. Lately, Ying and Gu [7] proposed a tool for performance-driven PGA package routing on multiple layers ceramic substrates. These routers [5-7] have a common distinguishing feature that they divided the substrate routing area into four separate

zones (namely top, bottom, left, and right zones). But these zones are not independent to each other, for examples, pad-to-pin nets may not belong to the same zone, or pins may be located at the borderline of two adjacent zones. Therefore, these routers cannot complete the routing task under a limited number of available layers when the input netlist becomes more complicated or there are serious crisscrosses among pad-to-pin nets on the routing area.

In this paper, we propose a windows-based routing tool for the PGA package based on the same model [4]. We cluster a set of grid array pins to form multiple rectangular rings on a substrate area. The structure and conceptual routing environment of this PGA package is shown in Figure 1. The objective of the package router is to connect each chip pad to the corresponding pin on the substrate area using less routing layers in the following: layer assignment, topological routing, and geometrical routing phases.

The remainder of this paper is organized as follows. Section 2 presents the problem formulation. Section 3 gives an overview of the package router. Details of the algorithms are discussed in Section 4. The experimental results are reported in Section 5. Finally, Section 6 concludes this paper and discusses some future research problems.

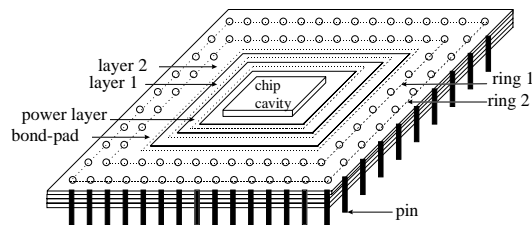


Figure 1. Routing environment of a PGA package.

## 2. Problem Formulation

As shown in Figure 1, a PGA package contains a central chip with a certain number of I/O pads distributed on the chip boundary, and has the same

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number of external pins to form a pin grid array around the chip. In addition, each I/O pad is wired to a pad on a substrate layer. The routing area is viewed like the moat space [8] between the edges of each substrate layer and the chip cavity, and multiple layers are sometimes required for the planar interconnections between the pads and the corresponding pins. All power and ground nets are routed on separated layers. We assume that every pin location is fixed and no pin assignment [9] is allowed because the package may be compatible with the pin locations of an off-the-shelf processor. Routing sequence for pad-to-pin nets is from the inner-most ring toward the outer-most ring and the wires may be routed in the kind of any angle. The routing result must satisfy the design rules constraint.

### 3. Overview of the Package Router

The design flow of our PGA package routing system is shown in Figure 2. The net lists include pad and pin descriptions as the input of the system.

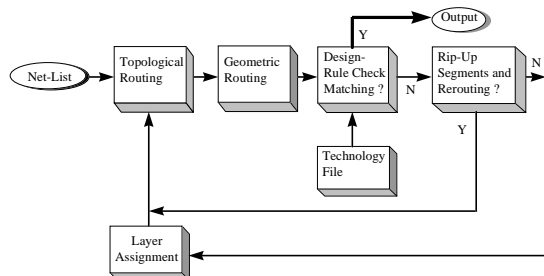


Figure 2. Design flow of the package router.

In the layer assignment phase, it is first to calculate the weights of each nets and then uses a simple comparison procedure to distribute nets onto suitable routing layers. The topological routing determines the topology paths for nets without any crossing and generates a planar sketch. After, the geometrical routing phase transforms the obtained planar sketch into an arbitrary-angle wiring and having the design-rule checking done. The technology file contains a set of design rules that state the parameters on the RLC (resistances, inductances, and capacitances) limits for each signal, the upper-capacity limit of wires passing through spacing between any two adjacent pins, and so on. We use a rip-up and rerouting step to change the routing direction of some segments if design-rule violation or routing cost has to be considered. The above phases will be performed repeatedly until the routing of all unrouted nets has been done.

### 4. Algorithm Descriptions

#### 4.1 Layer Assignment

The layer assignment phase is employed to distribute nets to two or more distinct layers when some existing nets cannot be routed on the current layer after the rip-up and rerouting step. In the topological routing phase, nets are routed from the inner-most ring to the outer-most ring in a multi-ring routing environment. Therefore, we must consider some routing factors like crossing number, detour length, and capacity in the layer assignment phase. For above reasons, let the weight of each net be  $W = \alpha V + \beta D + \gamma C$ , where  $V$ ,  $D$  and  $C$  represent the *inversion value*, *distance* and *capacity* respectively and  $\alpha$ ,  $\beta$  and  $\gamma$  are constants.

Using the notation of an inversion-table similar to Knuth [10], we can find two sets of  $V$ ,  $D$ ,  $C$  values and store them in a Right (R2L) inversion table and a Left (L2R) inversion table, respectively. Here, let  $(a_n, a_{n-1}, \dots, a_1)$  be a permutation of sorted data  $(n, n-1, \dots, 1)$ , then  $(d_n, d_{n-1}, \dots, d_1)$  represent the *right (left) inversion values* of  $(a_n, a_{n-1}, \dots, a_1)$ , where every  $d_i$  represents the number of elements located at the right (left) side of  $a_i$  and greater (less) than  $a_i$ . For instance, given a permutation (3, 2, 4, 1, 5), its R2L- and L2R-*inversion values* are (2, 2, 1, 1, 0) and (0, 0, 2, 0, 4), respectively. Again, assume pin  $i$  ( $P_i$ ) have an *inversion point* pin  $j$  ( $P_j$ ) at a ring, where an *inversion point* of net  $i$  in an R2L (a L2R) table is the first element greater (less) than  $i$  scanning from right to left (from left to right). The *inversion distance* of net  $i$  is defined as  $D_i = |m - n|$ , where  $m$  and  $n$  are the pin positions of  $P_i$  and its *inversion point*  $P_j$ , respectively. On the other hand, the *inversion capacity*  $C_i$  of pin  $i$  ( $P_i$ ) is equal to the number of nets which may pass through between  $P_i$  and  $P_j$ . That is  $C_i = |P_i - P_j| - 1$ .

Finally, we assign nets having minimum weights in the L2R table to one layer and nets having minimum weights in the R2L table to another layer. As shown in Figure 3, nets (8, 5, 7, 3) and (6, 4, 2, 1) have to be assigned to layers 1 and 2, respectively.

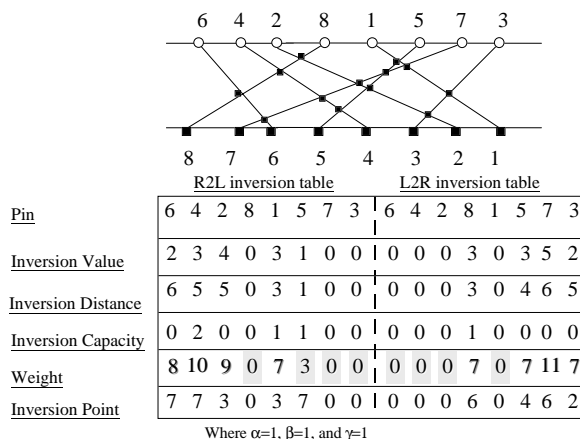


Figure 3. An example of weight calculation.

## 4.2 Topological Routing

In the direction-constrained topological routing phase, a ring is divided into several independent segments as shown in Figure 4 such that each segment can be chosen a better routing direction (toward left or right) to generate a shorter detour length. Each of independent segments will be transformed into a single row routing problem [11,12] by shifting and rotating the corresponding row of pads surrounding the chip to one side (left or right).

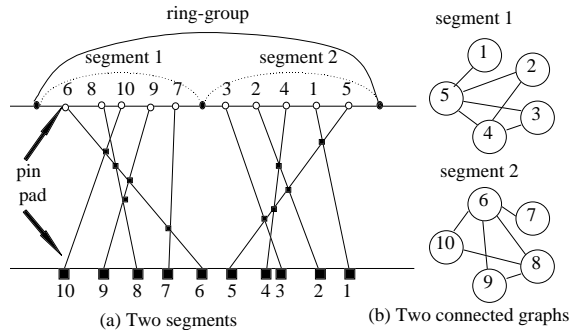


Figure 4. A ring divided into several segments.

The pin-side and pad-side interval diagram representation and how it corresponds to a single row are shown in Figure 5, where the wiring direction of a pin can be upward or downward while the wiring direction for pads can only be downward (after transformation). We use the term “direction-constrained” to mean that the wiring direction of a pad is only in one direction (while a pin has two directions) and must be away from the chip cavity for our PGA package routing. As a result, by means of shifting and rotating pads back to their original positions, we can obtain an arbitrary-angle planar topology layout, where the relative coordinates of pins and extra nodes (on the reference line) are recorded on each of ring-grid list (RGL). Due to space limitation, detailed discussion of this routing phase is omitted.

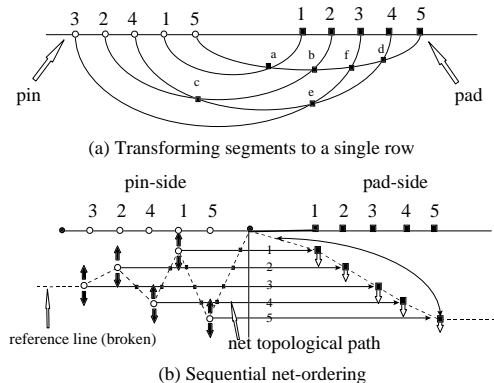


Figure 5. A segment routing transformed into a single row routing.

## 4.3 Geometrical Routing

Previous work by Dai [13] transformed a topological routing into a geometrical routing using rubber-band sketch. Our routing phase builds the detailed geometric connections between pads and external pins of a PGA package from a planar sketch obtained in the topological routing. Since the routing region can be partitioned into several sub-regions, we can create some vertical-grid lists to divide each sub-region into independent bin-grids, as shown in Figure 6. Whenever the path of any net passes through a vertical grid, insert its net number (as a redundant node) into the vertical grid list. Afterwards, each net in the bin-grid can be routed with a straight line using a river router [14] to connect its two terminals. Finally, the physical wiring paths of all of nets on routing area are made. Additionally, the rip-up and rerouting of a segment is performed only if we have to obey the design rules or to lower routing cost.

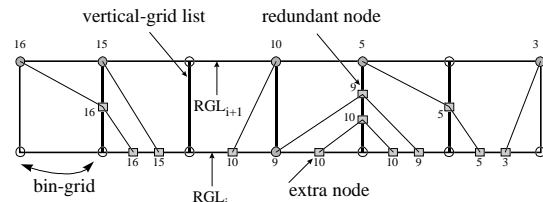


Figure 6. Partition a routing sub-region into several bin-grids.

## 5. Experimental Results

The PGA router has been implemented on a PC in Visual C++ language running Windows-98. Due to this type of benchmarks are not commonly available from the literature, some testing examples created by the authors are used to evaluate this router. The data were listed in Table 1 for eleven PGA packages. The wiring layout for a 200-pin PGA package (*chip\_11*) was plotted in Figure 7. As shown, our router can improve the common drawback of existing routers [5-7] that failed to deal with the cases where the pad and pin of the same nets are distributed on distinct routing zones (which causes the borderline problem). And it has provably undisputed advantage over manual designs in terms of routability and productivity.

## 6. Conclusions

We have presented an innovative windows-based routing tool for the PGA package routing on a multi-layer substrate. The router includes the following phases: First, the layer assignment phase determines nets to suitable layers. Second, the topological routing phase transforms the initial routing into a direction-constrained single row routing problem to obtain a non-crossing planar sketch. Finally, the

geometrical routing phase partitions the routing region into several independent sub-regions such that we can employ a river router to find an any-angle wiring layout for all nets. In future, we will extend this router to handle the routing problem of Ball-Grid-Array (BGA) package as proposed in [15] and apply it to a Multi-Chip Modules (MCM) environment.

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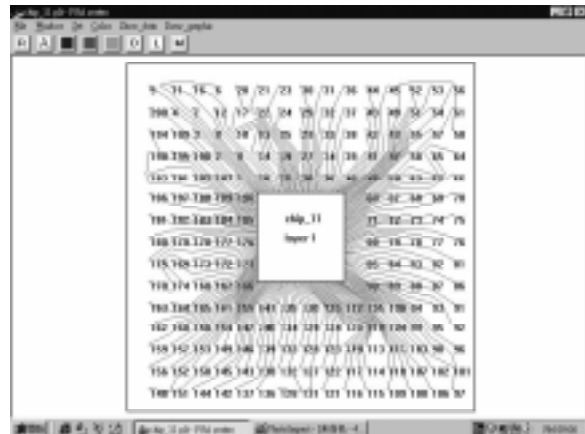


Figure 7. Single-layer routing result of a 200-pin PGA package.

Table 1. Routing results of distinct PGA packages.

| chip name | cavity size (pixels) | # nets | # rings | # routing layers | any-angle length (pixels) |
|-----------|----------------------|--------|---------|------------------|---------------------------|
| chip_1    | 104 x 104            | 84     | 3       | 1                | 8428                      |
| chip_2    | 104 x 104            | 84     | 3       | 1                | 9251                      |
| chip_3    | 110 x 110            | 84     | 3       | 2                | 8361                      |
| chip_4    | 110 x 110            | 144    | 4       | 1                | 12726                     |
| chip_5    | 110 x 110            | 144    | 4       | 1                | 14689                     |
| chip_6    | 110 x 110            | 112    | 4       | 1                | 14396                     |
| chip_7    | 110 x 110            | 112    | 4       | 1                | 14249                     |
| chip_8    | 110 x 110            | 200    | 5       | 1                | 28240                     |
| chip_9    | 110 x 110            | 200    | 5       | 1                | 23450                     |
| chip_10   | 110 x 110            | 200    | 5       | 1                | 23482                     |
| chip_11   | 110 x 110            | 200    | 5       | 1                | 23452                     |

Note: routing layers do not include power and ground layers.