Design Method of MTCMOS Power Switch for Low-Voltage High-Speed LSIs

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Abstract

The design of the power switch which turns on and off power supply to the logic gates is essential to low-voltage high-speed circuit techniques such as multi-threshold voltage CMOS (MTCMOS). This is because this switch influences the speed, area, and power of an low-voltage LSI. This paper describes the influences of the power switch on the circuit performance in detail, and proposes a systematic method for designing a power switch which takes them into consideration for the first time. The main feature of this method, called the average-current method, is the use of the average current consumed in an LSI to determine the power-switch size. This makes it easy for designers to determine the minimum size of the power-switch needed to satisfy the required speed, which results in minimizing the area penalty and the standby power. Useful analytical formula and the practical determination flow are also described. Measurement of an actual 0.25-μm MTCMOS/SIMOX 290-Kgate LSI operating at 1 V confirmed the effectiveness of this method. This method well estimated the required power-switch width, and as a result it reduced the area penalty and standby current by about 80% compared to the conventional design scheme.

1. Introduction

Various low-voltage circuit techniques have been proposed recently [1,2]. This is because lowering the supply voltage is the most effective way to reduce an LSI's power consumption. The multi-threshold-voltage CMOS (MTCMOS) circuit [1,3] is one such proposed technique. In the MTCMOS, high-speed operations at low voltages are obtained by reducing the threshold voltage (Vt) of a MOSFET for logic gates. Increased leakage current due to the low Vt MOSFET is reduced by placing high-Vt transistors between the logic gates and the power supply as a power-supply switch. By cutting these high-Vt transistors off during standby periods, the leakage current is drastically reduced. By this simple structure, the MTCMOS has been recognized as a candidate for the basic low-voltage circuit technique for the coming low-voltage era, and it has been applied to actual LSIs such as digital signal processors [3,4]. On the other hand, it has been pointed out that the high-Vt power-switch transistor degrades speed performance because of the voltage drop at the power switch [1]. One way to avoid this is, of course, to use a very large power switch. But a larger power switch increases a chip area. And it also increases the standby leakage current because the leak is proportional to the power-switch width. For these reasons, it is necessary to determine the power-switch width needed to satisfy the required speed performance for the MTCMOS LSI design. The design method in which the width of the cell-based logic-gate core is limited and the power switches are automatically placed at the both sides of the logic core has been proposed [1]. However, it was not discussed whether the total size of the power-switches placed like this is sufficient or not for various LSI operations. Therefore, it has not been easy for designers to determine the width of the power switch being tuned to their LSIs.

This paper first focuses on the influence of power switch on the speed performance, and describes a practical method for the design of an MTCMOS power switch. In this scheme, using the average current consumed in the LSI, designers can easily determine the power-switch width for the required speed specification, which results in minimizing the area penalty and the standby power. Effectiveness of this method is confirmed through the measurement of a 290-Kgates 1-V LSI. This method is not limited to only MTCMOS applications, but it can also be applied to other low-voltage circuit techniques using the power-switch concept [5,6].

2. Speed degradation mechanism in MTCMOS circuits

2.1 MTCMOS concept

The basic MTCMOS circuit is shown in Fig. 1 [3]. Power to the CMOS logic circuit is supplied via the "power switch" denoted as Q. In the MTCMOS circuit, the logic part is composed of MOSFETs with a low Vt of about 0.2 -0.3 V. A high-speed logic operation is

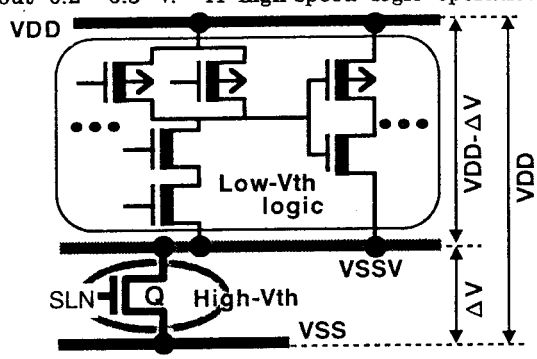


Figure 1. MTCMOS circuit.

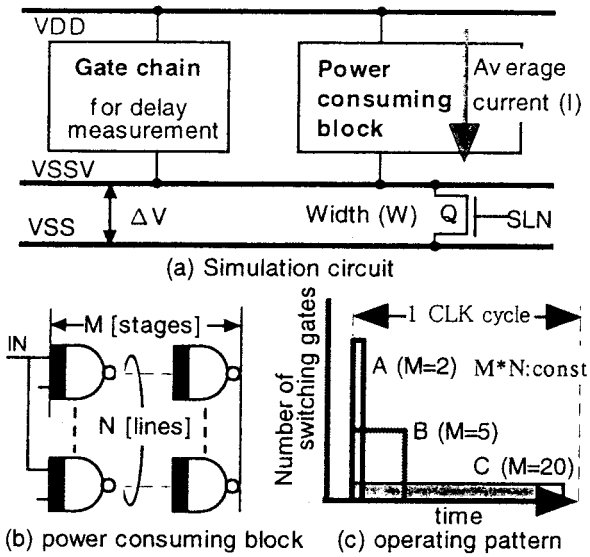


Figure 2. Simulation for MTCMOS delay.

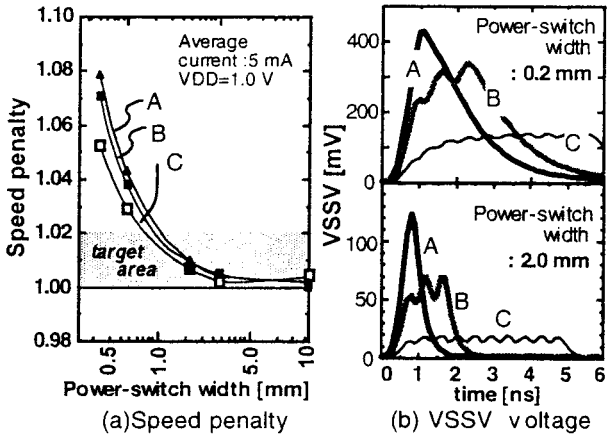


Figure 3. Simulation results.

possible even if the supply voltage is 1.0 V or less. To suppress the relatively large leakage current owing to the introduction of the low-Vt devices, a high-Vt MOSFET is used as the power switch Q, which is inserted between the true power line (VSS) and the virtual power line (VSSV). When the logic part does not operate, the turned-off power switch stops supplying power to the logic part, resulting in the leakage current being eliminated. The leakage current in this mode is proportion to the power-switch width. And in experiments, it was reduced by three or four orders of magnitude using the MTCMOS scheme [1,3].

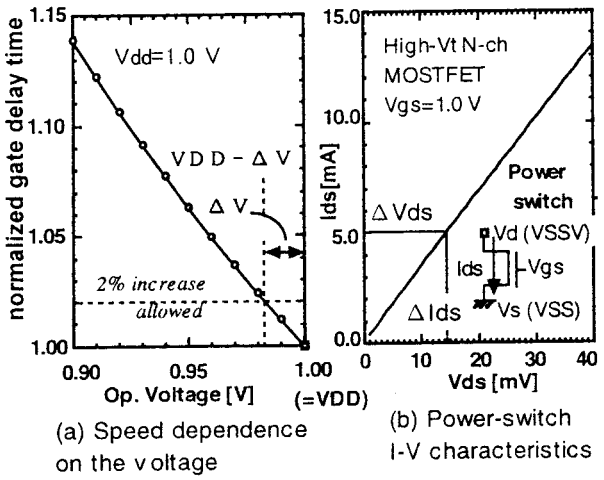
2.2 Delay-increase mechanism

As seen from Fig. 1, the effective supply voltage of MTCMOS circuits reduces to VDD-ΔV due to the voltage difference ΔV caused at the power-switch Q. Therefore, the speed of the MTCMOS circuits tends to be degraded compared with that of the fully low-Vt CMOS circuits, which are directly supplied with VDD. Figure 2(a) shows the simulation circuit to understand the influence of the power switch on the gate delay time. This circuit consists of two blocks. The first is the logic gate chain to measure the gate delay time. The second is the power consuming block that consumes the current, of which the average is denoted as "I". Figure 2(b) shows the power consuming block, where the M-stages and N-lines logic gates operate and generate a switching current and hence make the VSSV rise. One big concern when designing a power-switch is the influence of the circuit operation patterns. This is because different operation patterns are expected to vary current-flow patterns and thereby vary instantaneous ΔV behavior even if the average current is the same. Therefore, in this simulation circuit, various circuit operation patterns can be imitated by changing M and N, keeping the average current constant (N*M: constant). Examples of operation patterns are shown in Fig. 2(c).

2.3 Influence of operating patterns

Figure 3(a) shows the simulation results for the various operation patterns A, B, and C that are shown in Fig 2(c). The vertical axis is the MTCMOS's speed penalty. This represents how much the gate delay time increases by the voltage drop ΔV at the power switch, and this is defined as the ratio of the delay time of the MTCMOS circuit to the delay time of the low-Vt CMOS circuit which is directly supplied with VDD (about 10 ns for 24-stages 4-input NOR gate chain in this simulation). The larger the power-switch width is, the smaller the speed penalty is, since the power-switch width is inversely proportional to the voltage drop ΔV at the power switch.

Here let us consider the influence of the circuit operation patterns shown in Fig 2(c). In pattern A, lots of logic gates switch within a short period. In pattern C, on the other hand, relatively fewer logic gates continue to switch throughout one clock cycle. Pattern B is in-between. In the small switch-width region, the speed penalty for pattern A becomes larger compared with that for pattern C. The reason is explained by the VSSV wave forms shown in Fig. 3(b). Concentrated switching in pattern A instantaneously raises the VSSV to close to half of the VDD when power-switch width is 0.2 mm (the upper figure), resulting in the significant delay increase. When the power-switch width is 2 mm, on the other hand, the speed penalty for pattern A is almost the same as that for pattern C. This is because the instantaneous rise in the VSSV is well suppressed and the delay time can recover after the VSSV becomes close to VSS (after 2 ns in the lower part of Fig 3(b)). From these simulation results, we concluded that the speed penalty does not strongly depend on the circuit operating pattern if a power switch of a sufficient size is used and hence the speed penalty target is set sufficiently low (for example, less than 1.02 in Fig 3 (a)).



(a) Speed dependence on the voltage

(b) Power-switch I-V characteristics

Figure 4. Basic Data for the ACM.

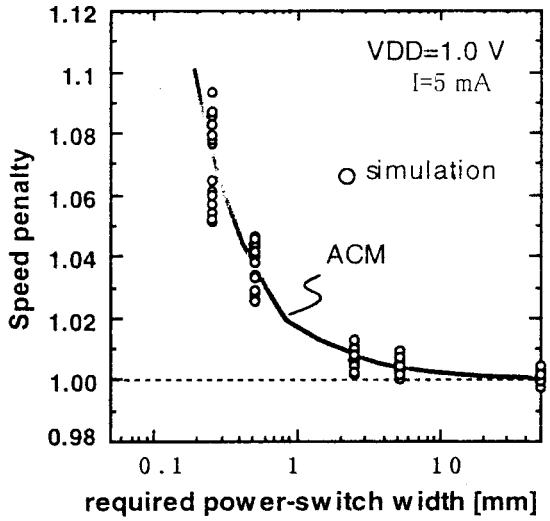


Figure 5. Comparison: ACM v.s. simulation.

3. Average Current Method for power-switch design

3.1 Concept

Here we propose the average current method (ACM) used to determine the required minimum power-switch size for the allowed MTCMOS speed penalty. With the ACM it is assumed that the current consumed in the MTCMOS circuit is constant, and hence the ΔV is also approximately constant. This assumption is appropriate because as concluded in the previous section the MTCMOS speed penalty does not strongly depend on the circuit operation patterns if the speed penalty target is set low. This makes it easy to analyze the speed penalty since the voltage drop at the power switch and gate delay time degradation are treated as a static phenomenon.

3.2 Detail of the ACM

The gate delay time of CMOS circuits at the supply voltage of VDD, τ [VDD], is approximately expressed by Eq. (1), where β is the drivability factor, C is the output load capacitance, α is 2 in the Shockley model, and Vtl is the low threshold voltage used for the logic gates. The effective operating voltage of the MTCMOS is VDD - ΔV taking the voltage drop ΔV at the power switch into account. It is assumed that the MTCMOS's gate delay time is equal to that of the low-Vt CMOS circuits with the VDD-ΔV power supply. Therefore, the MTCMOS speed penalty (MSP) becomes a ratio of the delay times at VDD-ΔV and VDD (expressed as Eq. (2)). The ΔV is expressed by Eq. (3), where R and I are, respectively, the power-switch resistance and the average current. R' is the normalized power-switch resistance and actual R is determined by the divided R' with the power-switch width (W). By rearranging Eq. (2) by substituting Eq. (3) into it, the MSP can be obtained as Eq. (4). From Eq. (4), we can determine the required power-switch width as Eq. (5) to guarantee the speed penalty of MSP, only if the current I and R' are prepared.

$$\tau[VDD] \propto \frac{C \cdot VDD}{\beta(VDD - Vtl)^{\alpha}} \qquad (1)$$

$$MSP = \frac{\tau[VDD - \Delta V]}{\tau[VDD]} \cong \left[\frac{VDD - Vtl}{VDD - Vtl - \Delta V}\right]^{\alpha - 1} \qquad (2)$$

$$\Delta V = RI = \frac{R'}{W} I \quad ; R' = R \cdot W \qquad (3)$$

$$MSP = \frac{1}{\left(1 - \frac{I}{W} \cdot \frac{R'}{VDD - Vtl}\right)^{\alpha - 1}} \qquad (4)$$

$$W = \frac{1}{1 - \sqrt[1-\alpha]{MSP}} \cdot \left(\frac{R'}{VDD - Vtl}\right) \bullet I \qquad (5)$$

3.3 Practical flow of the ACM

Equation (5) is convenient in roughly estimating the required power-switch width for each variable.

However, it includes some approximations, and actually it is not easy to determine a proper α value. To determine the power-switch size more accurately, therefore, it is recommended to obey the following flow using basic data: (a) delay tiime dependence on the supply voltage, and (b) I-V characteristics of the power-switch transistor.

Figure 4 (a) shows the delay-time dependence. As an example, let us consider the case where the MTCMOS speed penalty of 1.02 is allowed, which means the MTCMOS delay increases by 2% compared to the delay with low-Vt CMOS circuits supplied with the same voltage. In this case, the operating voltage has to be higher than 0.98 V, therefore the ΔV must be less than 20 mV. Figure 4 (b) show the power-switch's I-V characteristic near Vds=0. "R" is the resistance of the power switch, and is obtained using the slope of the I-V line in Fig 4 (b). In this example, R is about 3.0 Ω with the gate width of 1.0 mm, so that the R' is 3.0 Ω

Table 1. Technology and LSI characteristics.

Process Technology	0.25-μm MTCMOS/SIMOX 4-Metal, 1-Poly
Gate Length	0.24 μm/ 0.24 μm (NMOS/PMOS)
Gate Oxide Thickness	5 nm
Threshold Voltage (High)	0.18 V/ -0.22 V
(Low)	0.34 V/ -0.45 V
Chip Size	8 mm x 8 mm
Gate Counts	290 K
Supply Voltage	1.0 V
Power Consumption	210 mW (excluding I/O)

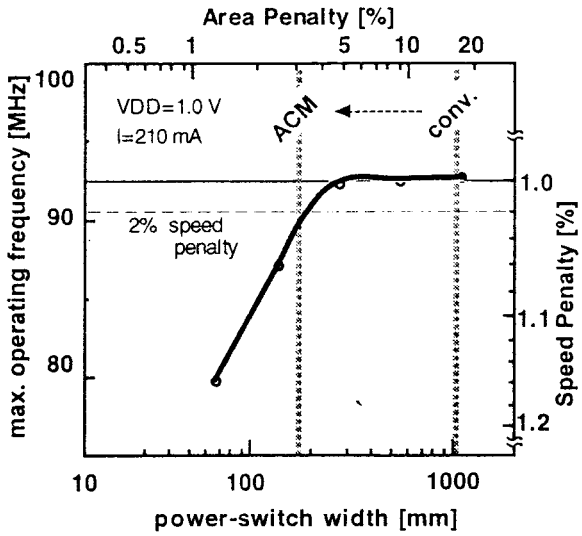


Figure 6. Measurement results

mm. By putting R' and ΔV into Eq. (3), the required power-switch size is determined to be Eq. (6). Figure 5 compares the results obtained from the ACM (Eq. (6)) and the SPICE simulations. Open circles indicate the simulation results from various operating conditions such as operation patterns, the switching probability, and the operating frequency. The results from the ACM and the simulations were in close agreement with each other, especially in the small MTCMOS speed penalty region, which is the usual target area for the power-switch design.

$$W = \frac{R'}{\Delta V} I = \frac{3.0[\Omega \cdot mm]}{20[mV]} * I[mA] = 0.15 * I[mm] \qquad (6)$$

4. Application to the1-V, 290 K gate LSI

We also confirmed the effectiveness of the ACM method by applying it to a 290-K gates communication LSI designed using 0.25-μm MTCMOS/SIMOX process. The details of the LSI, the process and the device technology are summarized in Table I. The number of power switches can be changed in order to observe the influence of the power-switch on speed performance. Figure 6 shows the measured speed performance and the corresponding speed penalty as a function of the power-switch width and the corresponding area penalty. Here the area penalty is defined as the ratio of the total sum of the gate width between the power switch and the transistors for logic gates. At 1 V, speed performance of over 90 MHz was obtained and it decreases in the narrow power-switch region. The vertical dashed line on the left side indicates the power-switch width determined using the ACM under the condition that the average current is 210 mA and the 1.02 speed penalty is allowed. It is confirmed that the 190-mm width estimated by the ACM agrees well with the measurement results. The vertical line on the right side indicates the power-switch width determined using the conventional method explained in the first section [1]. Compared to the 1000-mm width by the conventional method, the ACM reduces the area penalty from 17% to 3%. The standby leakage current when the power switches are cut off is also reduced from 6 μW to 1 μW by the ACM, because the leakage is proportional to the width of the power switch. These results demonstrate the effectiveness of the ACM.

5. Conclusion

Power switches are the important components in the low-voltage high-speed circuit technique, MTCMOS. This paper proposed the average current method (ACM) that is used to systematically determine the required minimum power-switch width. This method makes it easy for designers to automatically determine the power-switch width needed to satisfy the required speed using average current consumption. Useful analytical formula and the practical method for the ACM were explained. The effectiveness of the method was confirmed by comparison with the measurement results of an actual 290-Kgate communication LSI operating at 1 V. The described method will contribute to making it as easy to design an MTCMOS LSI as it is to design a CMOS LSI and to shortening the turn-around-time of low-voltage LSI production

Acknowledgments

The authors thank K. Takeya, and T. Kawanobe for their continuous encouragement. They also thank Y. Tanabe and M. Watanabe for the LSI design .

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