A Tool for Partitioning and Pipelined Scheduling of Hardware-Software Systems *

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Abstract

We present a tool for synthesis of pipelined implementations of hardware-software systems. The tool uses iterative hardware-software partitioning and pipelined scheduling to obtain optimal partitions which satisfy the timing and area constraints. The partitioner uses a branch and bound approach with a unique objective function which minimizes the initiation interval of the final design. It takes communication time and hardware sharing into account. This paper also presents techniques for generation of good initial solution and search space bounding for the partitioning algorithm. A candidate partition is evaluated by generating its pipelined schedule. The scheduler uses a list based scheduler and a retiming transformation to optimize the initiation interval, number of pipeline stages and memory requirements of a particular design alternative. The effectiveness of the tool is demonstrated by experimentation.

1. Introduction

The paper presents a tool for pipelined implementation of computation intensive-loop oriented hardware-software systems. Typical examples are digital signal processing applications like the JPEG algorithm.

Codesign Architecture: The tool assumes a fixed codesign architecture which contains a single general purpose software (SW) processor, a single hardware (HW) coprocessor and a block of shared memory. The shared memory is exclusive read-exclusive write. It is used for communication between tasks mapped to the SW processor and the HW coprocessor and also between two tasks mapped to the HW coprocessor. Communication between two tasks mapped to SW takes place through the local memory of the SW processor. We assume that the HW coprocessor cannot execute two tasks in parallel.

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Figure 1. Sequential versus Pipelined Design

System Description: The application is described as a directed acyclic graph (DAG) \( G = (V, E) \), where \( V \) is the set of tasks and the edge set \( E \), represents the data dependence between any two tasks. We assume that the DAG is executed a number of times inside a loop. Associated with each task \( v \in V \) are four quantities: \( v_{SW} \), the execution time of the task \( v \) on the general purpose SW processor, \( v_{HW} \), the execution of the task \( v \) in HW, \( v_{comp} \), the list of HW components (adders, subtracters, registers, etc) used to implement the task in HW and \( v_{p} \), the iteration index of the task. \( v_{SW} \) and \( v_{comp} \) of a task are obtained by using a high level synthesis tool[6]. Each edge \( e \in E \) has two quantities associated with it: \( e_{var} \), the number of variables transferred across a dependence and \( e_{d} \) the dependence distance. Iteration index \( v_{p} \) and dependence distance \( e_{d} \) are used to retime the DAG [5] for pipelined scheduling.

Motivating Example: Partitioning for pipelined implementation is significantly different from partitioning for sequential implementation. Consider the example in Figure 1. When partitioning for sequential implementation, the objective is to minimize the time for one complete execution of the DAG. The correspond-
The pipelined implementation is shown in the lower half of the figure. A pipelined schedule is characterized by its initiation interval, \( II \) which is the time difference between the start of two consecutive iterations of the steady state. For example the pipelined schedule in Figure 1 has an \( II = 365\text{ns} \). Given a partitioned DAG there exists a theoretical lower bound on the \( II \) of its pipelined schedule called the minimum initiation interval (MII). The \( MII \) in our case is determined by the number of resources in the codesign architecture and the execution times of the tasks. The execution time of a task \( \nu_{exe} \) is the sum of the task’s read time, run time on the resource that its been bound to and write time. The read (write) time \( \nu_{rdtime} \) (\( \nu_{wtime} \)) of a task \( \nu \) is the product of the number of variables read (written) by the task and memory read (write) time. If the sum of the execution times of the tasks bound to HW is represented by \( \tau_{hw} \), the sum of the execution times of the task bound to SW is represented by \( \tau_{sw} \), then the \( MII \) of a partitioned design is given by, 
\[
MII : \max(\tau_{hw}, \tau_{sw}).
\]
The objective of the partitioner is to bind the tasks to HW and SW so that \( MII \) is minimized subject to the area constraints. We present a HW-SW partitioner which uses a branch and bound approach to obtain optimal HW-SW partitions. We discuss techniques for generation of good initial solution and search space bounding. As the experimental results will show later, the initial solution is on an average within 9% deviation of the optimal. As a result we are able to effectively limit the search space and generate optimal partitions in a short period of time.

We evaluate a given partition by generating its pipelined schedule. We obtain pipelined schedules by retiming [5] and scheduling. Pipelining leads to an increase in shared memory requirements of the design. The total memory requirement of the pipelined schedule is 70 variables. The objective of the pipelined scheduler is to obtain a schedule with \( II \) as close as possible to \( MII \) with least number of pipeline stages and least increase in memory requirements.

The paper is organized as follows: in Section 2 we discuss previous work, Section 3 presents the tool, Section 4 discusses the experimental results and finally Section 5 concludes the paper.

2. Previous Work

In recent years a number of codesign systems for automatic partitioning and scheduling have been developed. Bjorn-Jorgensen et al. in [3] presented a critical path driven algorithm for mapping a task graph on heterogeneous multiprocessor architecture. In [7] Henkel et al. proposed a SW oriented HW-SW partitioner based on simulated annealing. Gupta et al. in [9] presented a HW oriented partitioning algorithm which moved parts of HW into SW while the timing constraint was satisfied. Kalavade et al. in [10] proposed a GCLP driven HW-SW partitioning algorithm. The algorithm used an adaptive objective function depending on a global criticality measure or local optimum measure. Niemann et al. in [13] presented an integer programming formulation for HW-SW partitioning. Our tool differs significantly from the existing approaches. All of them use a partitioning strategy and an objective function to satisfy the performance constraints for a sequential implementation. In contrast to the existing approaches our partitioner uses a branch and bound approach with a unique objective function aimed at minimizing the \( II \) of a pipelined codesign implementation.

Bakshi and Gajski in [1] describe a system level design space exploration approach for pipelined implementation of HW-SW codesigns. They use a list scheduling based pipelined scheduler [2]. In comparison to their approach we assume a fixed codesign architecture and take communication delays and shared memory requirements into account. They assume that the HW resource can execute two tasks in parallel, and therefore we cannot directly compare the two partitioners. List scheduling based pipelining techniques cannot choose which dependency should be converted from an intra loop dependency to a loop carried dependency. Iterative retiming and scheduling techniques can however select dependencies to be retimed. As a result we can explore a larger design space and optimize throughput, pipeline stages and shared memory requirements of the design.

Retiming to generate pipelined design is considered a generalization [8] of the classical transformation introduced by Leiserson et al [12]. [4] [15] are other approaches which use retiming and scheduling. Our retiming heuristic, RECOD differs from them since it tries to optimize the throughput, pipeline stages and shared memory requirements of a codesign application. It has been described in [5] and a comparison with existing approaches is also discussed. Other pipelining techniques based on loop unfolding [14] have the disadvantage of large memory requirements proportional to the unfolding factor of the loop. Our graph representation and problem formulation is similar to the paradigm of synchronous data flow machines [11]. However we have the extra dimension of area constraint that must also be satisfied.
3. Pipelined Codesign Implementation

The tool for partitioning and pipelined scheduling of HW-SW systems is shown in Figure 2. The partitioner tries to obtain a HW-SW binding whose $MII$ and area are less than the specified constraints. Although $MII$ takes HW and SW resource conflicts into account, it does not compensate for shared memory access conflicts and the extra communication delays that might occur. Therefore it is necessary to evaluate the performance of the partition by generating the pipelined schedule.

The tool first tries to find a schedule of the DAG with $MII$ as the time constraint. If it is unsuccessful it selects a dependency to be retimed. Intra loop dependencies (ILDs) with $e_k = 0$ constrain the scheduler. Retiming transforms an ILD into a loop carried dependency (LCD) ($e_k > 0$) which does not constrain the scheduler. The inner loop of scheduling and retiming continues till a successful schedule is obtained or all the dependences have been retimed. In the latter case we increase the initialization interval $II$ and try scheduling again. We set the increment factor to the maximum of the following two values: one time unit or one percent of $MII$. We exit the outer pipelined scheduling loop when the $II$ becomes greater than the time constraint. The design flow then returns back to the partitioner to generate a new binding. The outer loop of partitioning and pipelined scheduling continues till a successful schedule is obtained or the partitioner cannot generate a constraint satisfying binding.

Let the set $S = \{s_1, s_2, s_3, ..., s_n\}$ denote the set of all possible bindings of the tasks to HW and SW. For a particular binding $s_i \in S$, let $II(s_i)$ denote the achieved initialization interval of the corresponding pipelined schedule and let $\alpha(s_i)$ denote the total HW area of the binding. Let $\tau_{\text{constraint}}$ and $\alpha_{\text{constraint}}$ denote the time and area constraints specified by the user. We have the following four cases:

1. Both area and time constraint specified: In this case the tool searches for a binding $s_{\text{soln}}$ which satisfies the performance constraints, that is: $II(s_{\text{soln}}) \leq \tau_{\text{constraint}}$ and $\alpha(s_{\text{soln}}) \leq \alpha_{\text{constraint}}$. It returns the first solution which satisfies the constraints.

2. Only area constraint: In this case the tool searches for an optimal solution whose steady state executes in minimum time subject to the area constraint. Let $A$ denote the set of bindings whose area is less than the area constraint. Then the tool searches for a binding, $s_{\text{opt}} \in A$ such that: $II(s_{\text{opt}}) \leq II(s_i), \forall s_i \in A$.

3. Only time constraint: In this case the tool searches for a solution which satisfies the time constraint but has the least HW area. Let $T$ denote the set of bindings whose $II$ is less than the time constraint. Then the tool searches for an optimal binding, $s_{\text{opt}} \in T$ such that: $\alpha(s_{\text{opt}}) \leq \alpha(s_i), \forall s_i \in T$.

4. No area and time constraint: In this case the tool searches the design space for an optimal solution $s_{\text{opt}} \in S$ such that: $II(s_{\text{opt}}) \leq II(s_i), \forall s_i \in S$.

In the worst case our approach will exhaustively bind the tasks to HW and SW and execute with exponential time. Due to a good initial solution and tight search space bounding we are able to obtain optimal partitions for graphs having up to 30 nodes in a reasonable amount of time (30 mins). Since the application is modeled at a coarse level of granularity, 30 tasks are enough to model many applications. We provide a time out option for large graphs. The tool then returns the best solution that it obtains before the time out. As the experimental results will show later, the initial solution is on average within 9% deviation from the optimal. This implies that the partitions obtained by the time out option will also have good performance characteristics.

In the explanation given above (and in rest of the paper) we assume the optimal solution to be the one with respect to the partitioner. It is different from the global optimum which is with respect to both the partitioner and pipelined scheduler. The experimental results will show that although we use a heuristic scheduler the solution obtained by our tool is on average within 2.2% deviation of the global optimum.

3.1. Codesign Partitioner

The codesign partitioner uses a branch and bound approach with backtracking to explore the design space.
Algorithm Initial Solution
Input : DAG(V,E)
Output : level[] and bindings[] arrays
begin
  \forall v \in V \text{ calculate(suit(v))}
  \text{suit_array}[] = \text{tasks sorted in descending order of their suit.}
  \text{size} = |V|, \tau_{hw} = \tau_{sw} = i = k = 0, j = \text{size} - 1
  \text{while} \ (k < \text{size})
    \text{while} \ (k < \text{size} \ \text{AND} \ \tau_{hw} \leq \tau_{sw})
      \text{task} = \text{suit_array}[i], \text{level}[k] = \text{task}, \text{binding}[k] = hw
      \text{update_times}(\tau_{hw}, \tau_{sw}, \text{task}), k = k + 1, i = i + 1
    endwhile
    \text{while} \ (k < \text{size} \ \text{AND} \ \tau_{hw} \leq \tau_{sw})
      \text{task} = \text{suit_array}[j], \text{level}[k] = \text{task}, \text{binding}[k] = sw
      \text{update_times}(\tau_{hw}, \tau_{sw}, \text{task}), k = k + 1, j = j + 1
  endwhile
end

Figure 3. Algorithm for Initial Solution

Generation of good initial solution: We define the speedup measure for a task v as $v_{spm} = \frac{v_{sw}}{v_{hw} + v_{comm}}$, where $v_{comm}$ is the communication time when a task is bound to HW. We define the communication ratio for a task v as $v_{cr} = v_{sw}/v_{comm}$. Let $max_{spm}$ denote the maximum $v_{spm}$ for any task $v \in V$ and let $max_{cr}$ denote the maximum $v_{cr}$ for any task $v \in V$. In order to obtain a good initial solution we define the suitability for a task $v$ to be bound to HW as:

$$suit(v) = \begin{cases} \frac{v_{spm}}{max_{spm}} + \frac{v_{cr}K}{max_{cr}}, & v_{area}, \text{area constraint} \\ \frac{v_{spm}}{max_{spm}} + \frac{v_{cr}K}{max_{cr}}, & \text{no area constraint} \end{cases}$$

where $K$ was empirically found to be 0.5. In the above equation the first two terms try to balance the effects of speedup vis-a-vis increased communication time when a task is bound to HW. When an area constraint is specified we divide the sum of the terms by the area of the task to take the penalty into account.

Once we obtain the “suitability” of each task we sort the tasks in the descending order of their suitability. Then the first solution for the branch and bound algorithm is obtained by choosing one task alternatively from the front and back of the sorted list and binding them to HW and SW respectively. A task near the front (back) of the sorted list has a higher (lower) suitability and it is bound to HW (SW). During the generation of the initial solution we try to balance the following two quantities: $\tau_{hw} \approx \tau_{sw}$, where $\tau_{hw}$ and $\tau_{sw}$ are the running sums of execution times of tasks bound to HW and SW resources respectively. The MII for the initial solution $\sigma_{init}$, given by $max(\tau_{hw}, \tau_{sw})$ is minimized by keeping the two values balanced. The algorithm to generate the initial solution is shown in Figure 3. The search procedure for the branch and bound algorithm resembles a binary tree (see Figure 4). At a level $k$ ($0 \leq k \leq |V|$) in the search tree we make a decision about the binding of a particular task specified by the array level[k]. The initial binding of the task at the level $k$ is given by the array binding[k].

Sorting the tasks according to their suitability measure and then binding them in the above fashion to generate the initial solution has two important effects. First the initial mapping is a fairly good solution and it helps in limiting the search space of the algorithm. When the branch and bound algorithm begins its search (see Figure 4), it first exhaustively binds the tasks which are at the higher levels of the search tree. In comparison to tasks at lower levels (tasks t1, t5), the tasks at higher level (task t3) are not inclined towards either HW or SW implementation. Hence the second important effect is that the algorithm tries to obtain a solution by keeping the binding of tasks which are strongly inclined towards either HW or SW implementation fixed, and changing the binding of tasks which are not inclined towards either implementation. Such a search strategy coupled with a good initial solution leads to faster execution times of the algorithm.

Search space bounding techniques: We first explain the terms that are used in the discussion. At any time during the search process $s_{min}$ denotes the best solution found so far. Initially $s_{min} = \sigma_{init}$. During the search process we maintain three variables $\alpha_{hw}$, $\tau_{new,hw}$ and $\tau_{new,sw}$. At a particular level $K$ in the search tree, $\tau_{new,sw} (\alpha_{hw})$ gives the sum (estimated sum) of the execution times (areas) of the tasks which have been bound to HW from level 0 to $(K - 1)$. $\tau_{new,sw}$ is similarly defined. Let us assume that we are at level $K$, we have bound the task at level $K$ to both HW and SW and we are about to backtrack. We can associate two terms $\tau_{min,sw}$ and $\tau_{min,hw}$ with the task at level $K$. $\tau_{min,sw} (\tau_{min,hw})$ gives the sum of the exact execution times of the tasks which have been bound to SW (HW) from levels 0 to $(K - 1)$ in the solution $s_{min}$. The exact execution time of a task $v$, $v_{exact,exec}$ differs from $v_{exec}$ that we have defined earlier. $v_{exact,exec}$ is found from the pipelined schedule of $s_{min}$ and it takes the extra communication delays due to shared memory access.
conflicts into account \( v_{exec \_exec} \geq v_{exec} \). The initial values of \( t_{min \_sw} \) and \( t_{min \_hw} \) are infinity.

Consider the case when no constraints have been specified and we are trying to obtain a solution with minimum \( II \). Let us assume that we are at level \( K \) and bind the task to SW. Before we proceed to the level \((K+1)\) we check if the following two conditions are satisfied:

1. \( \max(t_{new \_hw} + v_{exec \_hw}, t_{new \_sw}) \leq II(s_{min}) \)
2. \( (t_{new \_hw} + v_{exec \_hw} \leq t_{min \_hw}) \) OR \( (t_{new \_sw} \leq t_{min \_hw}) \)

If the two conditions are not satisfied we backtrack and change the previous decision. We can similarly define two more conditions when the task is bound to HW:

3. \( \max(t_{new \_hw} + v_{exec \_hw}, t_{new \_sw}) \leq II(s_{min}) \)
4. \( (t_{new \_hw} + v_{exec \_hw} \leq t_{min \_hw}) \) OR \( (t_{new \_sw} \leq t_{min \_hw}) \)

In the presence of an area constraint we use the following condition along with the conditions 1, 2, 3 and 4 to limit the search:

5. \( Sum(\alpha_{hw}, v_{comp}) \leq \alpha_{constraint} \)

In the case that only a time constraint is specified we use the following three conditions to limit the search process:

6. \( Sum(\alpha_{hw}, v_{comp}) \leq \alpha(s_{min}) \)
7. \( \max(t_{new \_hw} + v_{exec \_hw}, t_{new \_hw}) \leq t_{constraint} \)
8. \( \max(t_{new \_hw} + v_{exec \_hw}, t_{new \_sw}) \leq t_{constraint} \)

When both area and time constraints are satisfied we use conditions 5, 7 and 8 to limit the search process.

During the search process besides using the above mentioned conditions, we bind tasks to HW or SW so that the two sums, \( t_{new \_hw} \) and \( t_{new \_sw} \) are balanced. Just like for the initial solution, balancing the two sums directs the search to a partition whose \( MII \) is small. We try to balance \( t_{new \_hw} \) and \( t_{new \_sw} \) only after we have generated the initial solution.

Area estimation: Since the HW processor cannot execute tasks in parallel, the HW tasks can share resources. The resources of the task \( v \), \( v_{comp} \) are classified into two types: those that can be shared (functional units and registers) and those that cannot be shared (controller and interconnect). The area estimator takes the union of the shared resources associated with all the tasks and then estimates the area due to them. The area associated with resources which are not shared is estimated by addition. The sum of the areas due to both type of resources is the total area occupied by the tasks bound to the HW processor.

Algorithm: The partitioning algorithm is shown in Figure 5. In the algorithm \( "P" \) denotes the level of the binary search tree. \( "first" \) is a boolean variable which is true when we reach a particular level for the first time and false otherwise. \( b1 \) and \( b2 \) specify the binding (HW or SW) of the task. Initially all the four parameters

```
Algorithm Partition(s,Tnew_hw,Tnew_sw,\alpha_{hw})
begin
if (i = |V|) /* Candidate Partition */
  II = pipeline_schedule()
  if (constraint_satisfied(II, \alpha_{hw})) return(1)
  else return(0)
endif
if (binding[i] = hw OR (NOT(first) AND Tnew_hw < Tnew_sw))
  b1 = hw, b2 = sw /* First bind task to HW then SW */
else
  b1 = sw, b2 = hw /* First bind task to SW then HW */
endif
  task = level[index]
  bind(task,b1)
  if (check() = T) S = Partition(i+1,Tnew_hw,Tnew_sw,\alpha_{hw})
else
  (S = 1) return(1)
  bind(task,b2)
  if (check() = T) S = Partition(i+1,Tnew_hw,Tnew_sw,\alpha_{hw})
else
  (S = 1) return(1)
return(0)
end
```

Figure 5. Branch and Bound Partitioner

in the call are zero. When \( i \) is equal to \(|V|\) all the tasks are mapped to HW or SW and we evaluate the candidate partition. When we traverse the graph for the first time we generate the initial solution according to the \( binding[] \) array. Otherwise we try to balance the two sums \( t_{new \_hw} \) and \( t_{new \_sw} \). The function \( bind() \) maps a task to HW or SW and updates \( t_{new \_hw}, t_{new \_sw} \) and \( \alpha_{hw} \). The boolean function \( check() \) as the name suggests checks if the conditions are satisfied.

3.2. Pipelined Scheduling

We evaluate the performance of a particular design alternative by obtaining a pipelined schedule. The pipelined scheduler takes resource conflicts due to SW processor, HW coprocessor and shared memory into account. It also takes communication delays into account. We use a list based scheduler and retiming transformation to obtain a pipelined schedule.

List based scheduler: The list based scheduler maintains three ready lists: a HW ready list, a SW ready list and a memory ready list. A task is added to the HW or SW ready list when all its predecessor tasks have been scheduled and completed their execution. A task is selected to be scheduled from the HW or SW ready list when the corresponding resource is free. The task is then considered to be in the ready state and it is added to the memory ready list. After it has been selected from the memory ready list the task does its read operation and runs on the assigned resource. After the task has completed its run state, it goes in to its write state and is again added to the memory ready list. A task finishes its execution after it is selected from the memory ready
list and scheduled to do its write operation.

The priority of a task to be selected from a ready list depends on its following three properties in descending order: mobility, variable difference and number of successors. The variable difference for a task $u$ is given by $\text{vardiff}(u) = r\text{dvar}(u) - w\text{rvar}(u)$, where $r\text{dvar}(u)$ ($w\text{rvar}(u)$) is the number of variables read (written) by the task $u$ from (to) the shared memory. A task with lower variable difference is selected to be scheduled before a task with higher variable difference. This priority function tries to reduce the shared memory requirement of the schedule [6]. A list scheduling algorithm performs better when it has more choice in the ready list [15]. Hence a task with more number of successors is selected.

**RECOD, A Retiming heuristic:** We do retiming when we are unable to schedule a DAG in the desired II. Memory required by LCDs is a lower bound on the memory requirement of the pipelined schedule [5]. By retiming we convert ILDs into LCDs leading to an increase in shared memory requirement. Our retiming heuristic [5], RECOD does retiming in two steps.

**RECOD Step 1:** In the first step RECOD selects a dependency which on retiming gives maximum freedom to the scheduler. Such a dependency is an ILD between tasks bound to heterogeneous resources and belonging to the critical path in the DAG. RECOD step 1 helps in limiting the number of pipeline stages by reducing the number of schedule-retiming iterations.

**RECOD Step 2:** In step two RECOD selects a set of dependencies (including the dependency selected in step 1) which on retiming result in the least increase in memory requirement. Given a dependency $\langle u, v \rangle$ to be retimed we can define the following three sets with respect to $u$:

$V_u = \{ \text{connected component to which } u \text{ belongs} \}$

$P = \{ w \in V_u \mid \text{there is a path from } w \text{ to } u \}$

$S = \{ w \in V_u \mid \text{there is a path from } u \text{ to } w \}$

$R = V_u - (P \cup S)$

In the second step RECOD partitions the set $R$ into sets $P$ and $S$ such that the number of variables transferred across the cut are minimized. RECOD retimes the DDG by using the following two equations:

$\forall u \in P, u_\lambda = u_{\lambda} + 1$

$\forall e = (u, v) \in E, u \in P, v \notin P, e_\delta = e_\delta + 1$

**4. Experimental Results**

We consider the HW-SW cosynthesis of the JPEG image compression algorithm. It is a loop oriented application and therefore ideal for pipelined implementation. We specified the algorithm as a DAG with 12 tasks. The hardware times and the component lists for each task were obtained for an ASIC implementation by using a high level synthesis tool. We then obtained pipelined cosynthesis implementations for the algorithm by specifying different constraints on the II and area. The results of the experimentation are in Figure 6. The results vary from the fastest implementation (in the top left) which occupies the maximum area to the slowest all software sequential implementation (bottom right). The tool took less than 2 seconds to generate a feasible solution for each of the design constraints. Moreover the pipelined schedules for all the partitions executed with MII, that is all were optimal pipelined schedules. This observation justifies the objective function of the cosynthesis partitioner. It also indicates that the pipelined scheduler is able to generate high quality schedules.

Our next four experiments aimed at evaluating the run time of the tool, establishing the quality of the initial solution and evaluating the overall approach. Due to the lack of accepted benchmarks in cosynthesis area, we conducted the experiments with 50 randomly generated task graphs. The graphs had a varying number of nodes (upto 30), different depths and different connectivity. The plots of the results (Figures 7, 8, 9, 10) are divided into 5 regions: the first region has graphs with 10 nodes each, the second region has graphs with 11-20 nodes and the third region has graphs with 21-30 nodes.

We evaluated the run time of the tool by invoking it for each of the task graphs and obtaining an optimal solution under no constraints (see Figure 7). The maximum run time of the tool was 30 minutes for a graph with 30 nodes. A low run time was possible because of the good quality of the initial solution and the search space bounding techniques. In the second study we analyzed the quality of the initial partition generated by the tool. We calculated the percentage deviation of the initial partition from the optimal partition for various graphs (see Figure 8). The average percentage deviation was 8.4% with the maximum being 27%. In the third study we plotted the number of solutions generated by the partitioner before it found the optimal one.
Figure 8. Results of Experiment 2

Figure 9. Results of Experiment 3

Figure 10. Results of Experiment 4

(see Figure 9). The average number was found to be 5.62 and the maximum number was 17. Studies 2 and 3 demonstrate the superior quality of the initial solution. Therefore for large graphs we can use a timeout option for the co-design partitioner and still have a high degree of confidence in the quality of the design solution.

Finally in the fourth study we compared the solutions obtained by our tool against the minimum MII that was obtained by the partitioner during design space exploration (see Figure 10). The minimum MII is a lower bound on the global optimum solution for a particular task graph. The final solution is on an average within 2.2% of the global optimum. This result validates our overall approach. We are able to generate high performance designs because of the superior quality of the retiming heuristics.

5. Conclusion

The approach can generate optimal partitions for task graphs with up to 30 nodes within a short period of time. Further, the obtained designs are very close to the global optimum. The limitation of the tool is its inability to handle large task graphs (greater than 30 tasks) in a reasonable time. It also assumes a simplistic co-design architecture which cannot execute two HW tasks in parallel. Future work will involve extending the technique to overcome these limitations.

References

