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Proceedings

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Message from the Program Chair

On behalf of the ISSS’98 Organizing and Technical Program Committees, we would like to welcome you to the 11th International Symposium on System Synthesis, held in Hsinchu, Taiwan, Republic of China, on December 2–4, 1998.

ISSS is a major international forum presenting emerging techniques for the system-level design and synthesis of computing systems. Having begun as the International Workshop on High-Level Synthesis in the mid-1980s, it attracts leading design automation professionals from around the world. The growing acceptance of commercial synthesis tools, and the unified view of both hardware and software that such tools enable, have led to the symposium expanding such that it now covers system-level synthesis, hardware/software codesign, programmable (multi-)processor-based design, architectural and high-level synthesis, system-design experience and methodologies, embedded and real-time system software, synthesis for low power and testability and verifiability.

This year we received 63 submissions from 17 countries. The papers were distributed and subjected to “blind” reviews by an international panel of 33 experts in the field. Each paper was evaluated by five to seven reviewers. The Technical Program Committee used these reviews, along with their own expert opinions, to select the very best 18 regular papers and 6 poster presentations.

ISSS’98 also features four invited talks by leading industrial and academic experts on System-On-A-Chip and IP reuse topics. In addition, a panel session has been set up to discuss the direction and viability of IP-based design methodologies.

Finally, I would like to thank all of the organizing committee and staff members who contributed to the success of this symposium. Foremost, I would like to thank our secretariat Ms. Shu-Jane Lee for organizing the symposium. I would like to thank staff members Matrix Heish, Tony Cheng, and Peng-Cheng Kao for their contribution in handling the electronic paper submission process, the review process, and setting up the web page. I would also like to thank our general chair Francky Catthoor and previous general chair Frank Vahid, both of whom provided us with very useful information about past years’ events. Last, but not least, I would like to thank the Technical Program committee for their tremendous efforts in selecting this year’s excellent program.

Welcome to Hsinchu, Taiwan, and enjoy ISSS’98.

Allen C.-H. Wu
Program Chair
Invited Talks

Is IP Business Hype or Reality?

D. D. Gajski
University of California at Irvine, USA

Abstract: Selling and using IPs seems to be the perfect solution for improving design productivity. However, IP business models may not have adequate infrastructures with which to flourish. This talk will elaborate on new design styles, modeling guidelines, methodologies, and CAD tools needed for successful reuse.

Issues in Embedded DRAM Development and Applications

Doris Keitel-Schulz
Siemens Research and Development, Germany

Abstract: The term system-on-silicon has been used to denote the integration of random logic, processor cores, SRAMs, ROMs, and analog components on the same die. Until recently, however, one major component had been missing: high-density memories such as DRAMs. Today’s integration densities are beginning to allow the integration of significant amounts of DRAM memory. Embedding DRAM can therefore be considered a key technology for certain applications such as data buffering, picture storage, and program/data storage. Fast on-chip buses between DRAM and logic, low-power dissipation, fewer pins, higher integration density and optimized memory structures are among its major advantages. In this talk we discuss some of the challenges associated with embedded DRAM design in greater detail.

Processor Architectures and Compilers for Systems on Chips

Monica Lam
Stanford University, USA

Abstract: As it becomes possible to integrate an entire system on a chip, the processor architect is presented with an unprecedented opportunity to tailor the processor to the application at hand. To fully realize the potential of this technology, it is critical for us to be able to quickly produce an optimized processor design and associated programming tools. Languages and compilers have an important role in the revolution of processor IP in ASIC designs. Many of the advanced architectural ideas (parallelism, memory subsystem optimizations) originally developed for high-end processors are directly applicable to this environment. They often require nontrivial compiler support. Opportunities for application-specific optimizations can be exposed by means of more expressive programming languages. Finally, program analyses can extract program characteristics that can be used directly in guiding the architecture customization process.
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