A Three-Port Adiabatic Register File Suitable for Embedded Applications

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Abstract

Adiabatic logic promises extremely low power consumption for those applications where slower clock rates are acceptable. However, there have been very few adiabatic memory designs, and any circuit of even moderate complexity requires some form of RAM. This paper presents a register file implemented entirely with adiabatic logic, and fabricated using a 1.2 μm CMOS technology. Comparison with a conventional CMOS logic implementation, using both measured and simulated results, indicates significant power savings have been realised.

1 Introduction

RAM is an important component of any circuit of significant size. It can also make a significant contribution to the power consumption of such circuits due to the need to drive large capacitances in address, word, and bit lines. Slowing the clock rate can decrease the power consumption, but with conventional CMOS circuits, the relationship is linear, and the reduction in speed must be considerable to have any real impact. In adiabatic systems, however, the relationship between power and speed is quadratic [1]. This is accomplished by both reducing the power dissipated by each individual FET, and recycling the charge stored at each node in the circuit.

To realise any significant power savings, however, adiabatic logic must operate at clock rates much slower than the maximum possible for a given fabrication technology. Typically, this means operating in the range 1–20 MHz. In some embedded applications like biomedical implants [3], such clock speeds are acceptable, and the increase in battery life through lower power consumption makes adiabatic logic attractive.

The use of adiabatic and energy recovery techniques in memory design is not new. The first published design by Somasekhar, Ye and Roy describes a quasi-static adiabatic RAM cell [8]. The circuit is based on a conventional 6T cell, but uses a complex adiabatic clocking scheme with different offsets and swings to generate all signals and power supplies. Simulations of a 64×64 array using a 1.2 μm technology show 84% energy recovery for reads and 85% for writes.

Dennard and Frank take a different approach, describing a technique for reducing the power consumption of DRAMs by adiabatically switching the bit lines [5]. As the bit lines of a DRAM are highly capacitive, by charging and discharging them adiabatically the charge stored on those lines may be reclaimed and recycled, leading to power savings.

Tzartzanis and Athas propose a similar technique for static RAM, replacing all latches and drivers in a conventional SRAM with energy recovery versions [9]. Simulations for a 256×256 SRAM array show energy savings of between 59% and 76%, at 200 MHz, over a conventional implementation.

Moon and Jeong go one step further, using energy recovery logic for all circuits in a register file except for the RAM cells [7]. Power savings of approximately 70% at 5 MHz are claimed for a 32×32 two port register file implemented in a 0.8 μm technology.

This paper describes a three-port register file implementation using only adiabatic logic, the natural progression from previous adiabatic/conventional hybrids. The sole use of adiabatic logic allows significant power savings, and ready integration into larger adiabatic systems. The performance of a 8×16 register file is then compared with that of a conventional implementation using simulated and measured results.

2 Memory Cell

Figure 1 illustrates a conventional implementation of a three-port memory cell by Chao and Wooley [2]. Devices M1 through M4 provide a storage element with negligible static power dissipation. Two pairs of nFETs, M5/M6 and M7/M8, allow reading from the cell by selectively discharging the bit lines, and the pair M9/M10 allows data to be written to the cell.

Figure 2 is the adiabatic memory cell used in this implementation. It is similar to the conventional memory cell, except that it is powered by the clock like all adiabatic circuits, and the cell outputs are not directly connected to the data buses.

Devices M1 through M4, M9, M10, M13, and M14 form a 2N-2N2P logic gate [4]. To write a value to the cell, the clock is ramped down to ground, reclaiming charge stored in the cell. The write word line is then asserted and data placed on the Wbit lines. Ramping the clock up again causes the cell to take on a state dependent on which pair of nFETs, M9/M13 or M10/M14, provide a path to ground. After the

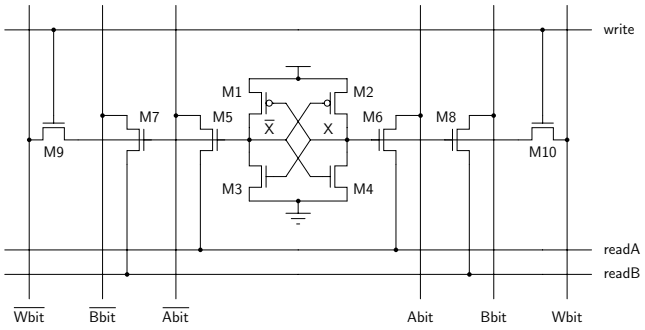

Figure 1: Conventional three-port memory cell

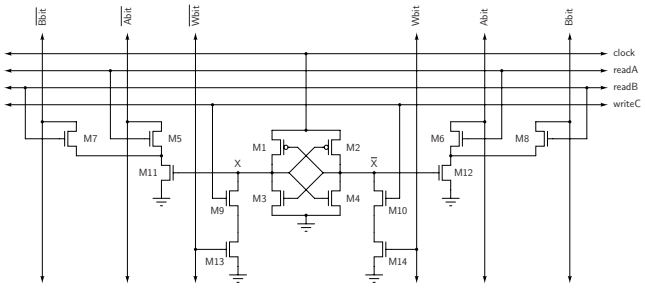

Figure 2: Memory cell used in the register file

clock has reached V_{dd}, the data and write signal may be removed, and the cell will maintain its state indefinitely.

The worst case power consumption occurs when the cell state is toggled. As M1/M2 cease conducting when the clock line drops below V_{th}, a charge of CV_{th} will remain on one of the storage nodes (where C is the node capacitance). If the cell state is toggled, this charge is dumped to ground, resulting in an energy loss of ${CV_{th}}^2$. This, however, is considerably less than the ${CV_{dd}}^2$ energy loss of a conventional SRAM cell.

3 Write Decoding

For the memory cell to retain its value, the clock must be held at V_{dd} when the cell is not selected for writing. To accomplish this, the write word decoder is modified to gate between the clock and V_{dd} as shown in Figures 3 and 4.

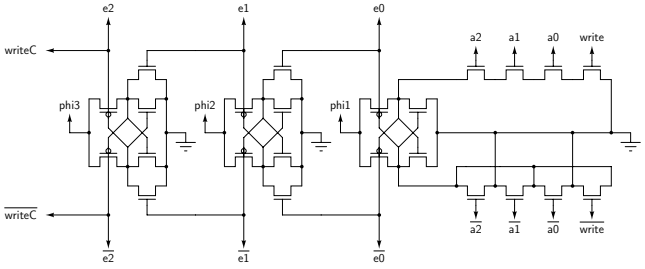

Figure 3: Adiabatic write word decoder

The write word decoder is a simple decoder followed by two buffers. This allows the decode signal to be made available across three clock phases. These signals are used to drive the clock gating circuitry, which ensures that the clock

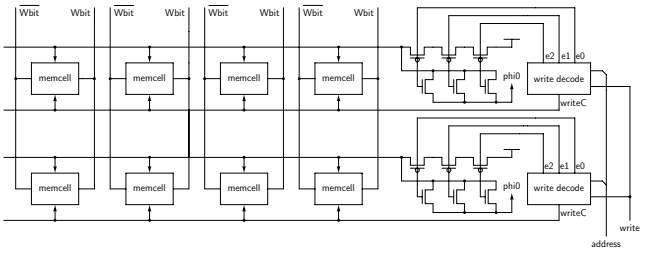

Figure 4: Full write word decoding circuitry

is either connected to V_{dd} through three pFETs, or to the power clock (phi0) through one of three nFETs (Figure 5).

Full transmission gates cannot be used (as it is not possible to generate fully complementary signals), and so the potential across the pFETs is V_{th} when they are switched on. This results in a non-adiabatic transition from $V_{dd} - V_{th}$ to V_{dd}, and a slight increase in power consumption over an ideal adiabatic implementation.

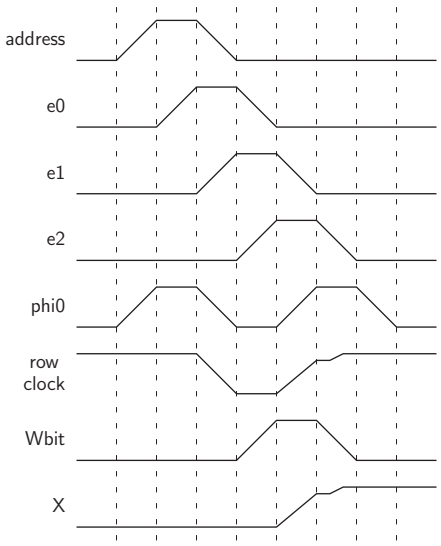

Figure 5: Write operation timing

4 Read Decoding

A simple decoder is all that is required for the read decoder, as illustrated in Figure 6. Because the gate must be able to sink the charge stored on the entire word line, decoders in large register files can be slow due to the number of nFETs in the discharge path. To combat this problem, a buffer may be added at the output, shortening the discharge path to one nFET at the expense of an extra quarter cycle of latency. Figure 7 illustrates the read operation timing.

5 Read Data Output

In place of the sense amplifier used in conventional RAM circuits, this implementation uses an OR gate, with the evaluation tree distributed along the length of the bit lines. An additional nFET connected to the complementary output ensures the gate reaches a sensible state when no read is performed. The circuit is illustrated in Figure 8.

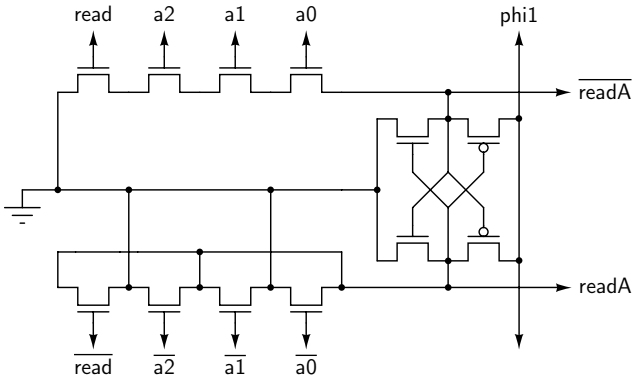

Figure 6: Adiabatic read word decoder

The bit lines in a RAM are typically the most capacitive. Large FETs are therefore required in the cross-coupled portion of the gate to reduce losses associated with charging these lines from the clock. As a consequence, the nFETs in the evaluation branches may be relatively small due to the large gain of the cross-coupled FETs. This helps keep the area of the memory cells reasonable.

As with the read word decoder, the output should be buffered to help minimise the current sinking requirements of the evaluation branches.

6 Integration

The register file is powered by a four-phase clock, with phi1 lagging phi0 by 90°, phi2 lagging phi1 by 90°, and phi3 lagging phi2 by 90°. While a trapezoidal waveform is ideal, a sinusoidal clock may be used with only a slight increase in power dissipation.

All address and read/write signals must be valid during phi1, ie. may only change when phi1 is low. The data to be written must be valid during phi3, although this implementation uses buffering to synchronise that data with all other input signals. The data read is valid during phi3, with all operations performed within one clock cycle.

7 Implementation and Results

The circuits presented here were used to implement a 8-word×16-bit 2R1W register file which was fabricated using the MOSIS 1.2 μm CMOS process. To provide a basis for comparison, a similar register file was implemented with conventional CMOS logic. The conventional circuit, generated from symbolic layout, was provided by N. Weste of Macquarie

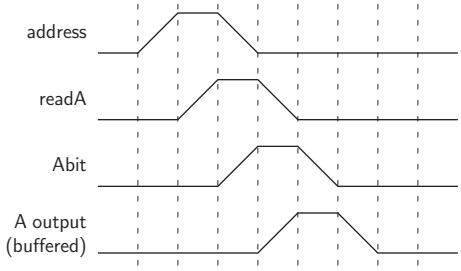

Figure 7: Read operation timing

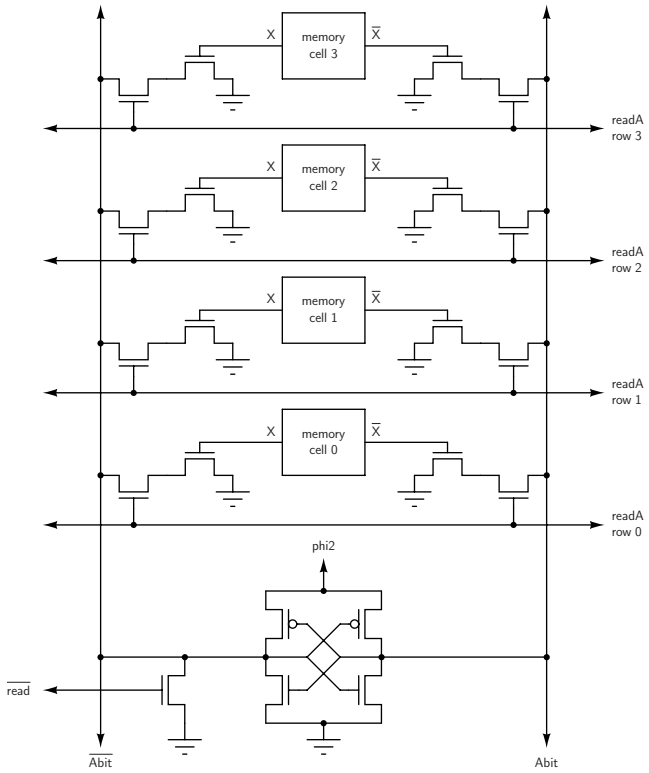

Figure 8: Adiabatic read output circuitry

University. It was then compacted by hand to ensure a fair comparison with the adiabatic implementation, which was laid out geometrically. Figure 12 is a photomicrograph of the fabricated chip.

The final size of the adiabatic circuit is 644×1300 μm, comprising 2876 devices (588 pFETs). By comparison, the conventional implementation is 880×883 μm, and uses 2264 devices (888 pFETs). Despite the larger number of devices, the adiabatic circuit requires less than 10% more silicon. This is due to the smaller number of pFETs, and the corresponding relaxation of n-well requirements.

Figure 9 shows the power consumption for both circuits for a range of clock frequencies and V_{dd}=5 V. These results

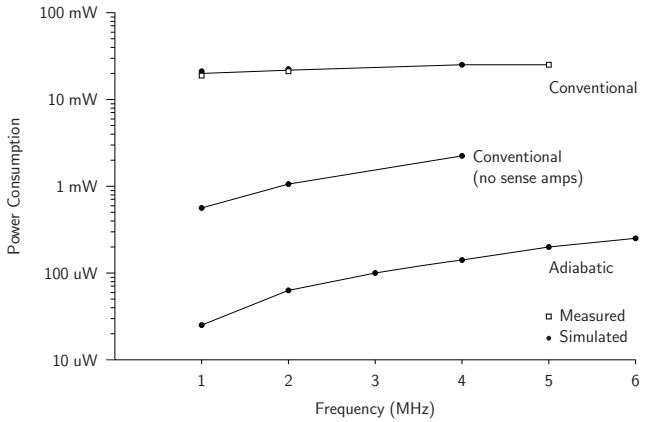

Figure 9: Power consumption versus frequency

Function	Conventional	Adiabatic
Buffering	336 μW	8.6 μW
Read Decoding	139 μW	5.2 μW
Write Decoding	62 μW	4.5 μW
Read Output	20.7 mW	5.3 μW
Memory Cells	31 μW	4.2 μW

Table 1: Power consumption at 1 MHz (V_{dd}=5 V)

are based on a 50% level of activity, ie. 50% probability that the output of a gate will change. The activity level in practice, and hence the actual power consumption, will likely be much lower. It can be seen that the measured results for the conventional circuit closely correspond to the simulation results. The results for the adiabatic circuit are from simulation only, as measured results were not available at the time of writing.

Table 1 provides a breakdown of the power consumption of the circuits by function. As can be seen, the power consumption of the conventional sense-amps swamp the results for that implementation. The reason for this can be seen in the circuit schematics of Figures 10 and 11. When the clock is high, the 20/1 nFET in the sense-amp precharges the bit line to V_{dd}. If the value stored in the memory cell is high, and that cell is selected for reading, then the bit line is dragged low through 2/1 and 5/1 nFETs. This results in a short circuit current of approximately 500 μA with 50% duty cycle for each bit in the word being read which is high. Although this sense-amp circuit is useful in the original application (the register file in a fast RISC core), it is not particularly suitable for a low-power low-speed application. (Note that the problem could be fixed by ANDing the word select with the clock's complement.) For this reason, Figure 9 provides results for the conventional circuit without the sense-amp power consumption.

Even when the conventional sense amplifiers are ignored, the adiabatic circuit produces impressive power savings compared to the conventional implementation. These savings range from 85% for the memory cells, through to more than 90% for the decoders. As the charge stored on the bit and word lines is being recycled, such significant power savings are to be expected of the decoders and read data output circuitry.

In simulation the conventional circuit operated to more than 10 MHz and the adiabatic circuit, designed to operate at 5 MHz, to just over 6 MHz. The adiabatic circuit can operate at higher clock frequencies by using wider FETs in the clock gating circuitry and by increasing the drive of the decoders. Note that measured results are limited by the failure of the I/O pads, not necessarily by failure of the circuits.

If the additional losses associated with the energy recycling clock are considered (which can be as low as 10–15% [6]), total power savings of more than 80% over conventional SRAM designs are still possible.

8 Summary

To realise their full power-saving potential, adiabatic systems require some form of adiabatic memory. We have demonstrated a register file implemented entirely with adiabatic logic, a natural progression from other hybrid energy-recovery memory systems.

This circuit has produced significant power savings over a similar implementation using conventional CMOS logic. Savings are particularly notable where highly capacitive buses are driven, as in the read data output, and row decoders.

This work shows that in applications where slower clock rates are acceptable, power savings in the order of 80% are possible in memory circuitry through the use of adiabatic techniques.

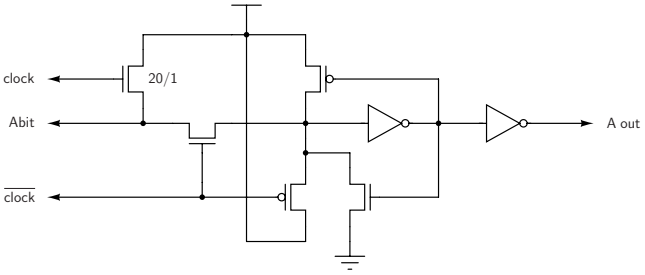

Figure 10: Sense amplifier used in conventional circuit

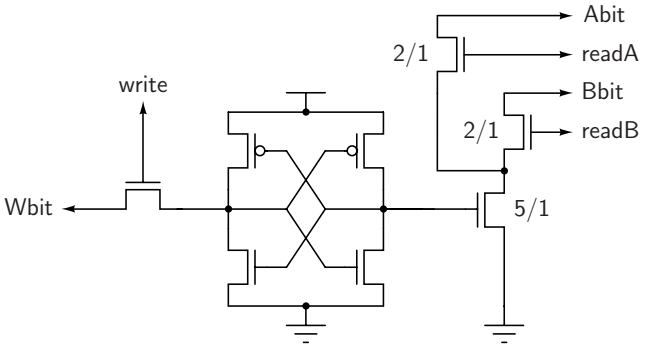

Figure 11: Memory cell used in conventional circuit

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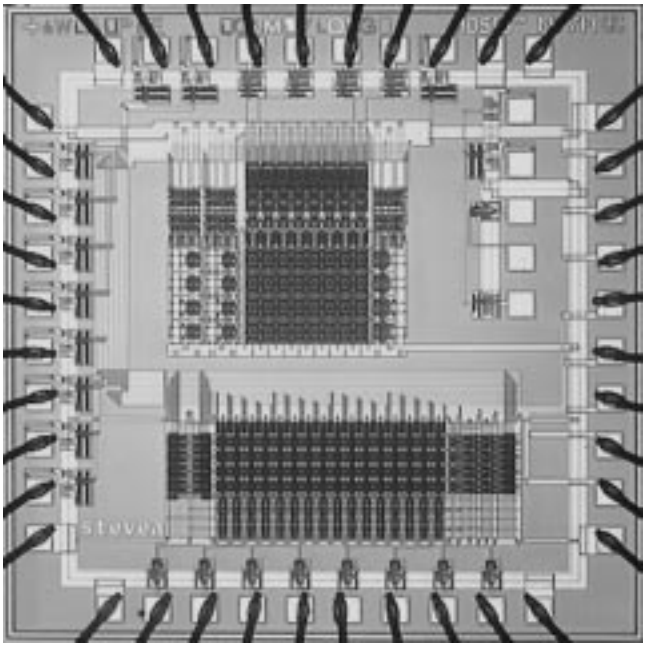

Figure 12: Photomicrograph of the conventional (top) and adiabatic (bottom) register files

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