Low-Power Miniaturized Information Display Systems

Michael Bolotski
The MicroDisplay Corporation
3055 Research Drive
San Pablo, CA 94806
+1 (510) 243 9515
misha@microdisplay.com

Phillip Alvelda
The MicroDisplay Corporation
3055 Research Drive
San Pablo, CA 94806
+1 (510) 243 9515
alvelda@microdisplay.com

1. ABSTRACT

This paper discusses low power issues in the design of miniature information display devices built on silicon substrates.

1.1 Keywords

LCOS, microdisplay, power, field-sequential color

2. INTRODUCTION

The capacity for portable devices to process and communicate information is growing exponentially, particularly with the advances in wireless technologies. One of the critical factors limiting a pervasive personal information infrastructure is the ability to display the massive and growing amount of available information on portable systems. Several new technologies have matured over the last two years to provide new high-resolution display capabilities in portable systems commensurate with what is currently available for the desktop. Plasma displays, field-emission displays, organic LEDs, electro-luminescent displays, and new generations of traditional liquid crystal displays continue to evolve lower-power architectures yearly. One particularly attractive family of new display technology has grown on the foundation of traditional CMOS substrate fabrication infrastructure to offer the high integration and low-power circuit capabilities already developed for the microprocessor and memory markets. CMOS backplanes have been used to drive displays with many different optical materials patterned atop the silicon, ranging from micro-machined mirrors, to organic light emitting diodes, to electro-luminescent phosphors. Of them all, liquid crystal materials laminated on silicon (LCOS) technology promises to provide the most compact, inexpensive, low-power, and high-performance microdisplays to enable portable information systems. This discussion addresses the power-dissipation issues associated with miniature display architectures, VLSI techniques for driving optical materials efficiently, and conversion of imagery in analog and digital formats.

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Display systems consume power in three key subsystems: the silicon-based light modulator, the drive circuitry, and the illuminator. The discussion omits the illuminator design issues and concentrates on the light modulator integrated circuit. The discussion first presents principles of operation and fundamental architectures of entire miniature information display system solutions, in addition to the architecture of new VLSI backplanes. Issues associated with on-chip signal distribution and driving optical materials are described next, as they determine the display drive scheme, followed by a presentation of several improvements over the basic architecture. Once the architecture and drive schemes are understood, we discuss the interaction between image properties, drive schemes, and power consumption. Finally, the power requirements of creating a color displays are presented in conjunction with conclusions about upcoming digital display standards and wireless infrastructures.

3. Light Modulator Power

As an array of miniature capacitors, the smaller a display, the less power it will dissipate. This means that the first displays to run full-motion high-resolution video for any appreciable amount of time on battery power will be very small, likely with magnification optics to create a viewfinder, as in camcorders and digital cameras. Of all the above-mentioned miniature display technologies, new approaches to marrying liquid crystal materials with CMOS backplanes offer the lowest power alternatives to high-resolution portable displays. Nonetheless, the architectural and information display issues described below apply to any VLSI system designed to drive an optical switching material.

LCOS displays consist of a three-element stack: the silicon backplane, the liquid crystal material, and a transparent conductive cover. The brightness of a display at a particular pixel is controlled by applying a voltage across the LC material and between the pixel electrode and the conductive glass cover. In a silicon process, the pixel electrode is built using the topmost metal layer on the chip. Thus, controlling the voltage on the pixel electrode determines the pixel brightness.

3.1 On-chip signal distribution

The signal distribution architecture controls how the voltages are delivered to the pixel electrodes. The incoming

video signal drives a video wire that runs across the top of the chip. Each pixel column is connected to the video wire via an analog switch. The switches are controlled by a shift register that typically contains a single high bit, which propagates along the shift register, connecting one column at a time to the video wire. All pixels in the selected row are connected to their column wires at a time, as determined by the vertical shift register. Thus, as each analog pixel value is placed on the video wire, it is sampled by the column wire and the currently active pixel on the column wire. After all pixels in a row have been loaded, the vertical shift register advances to the next row and the process repeats.

Most of the power dissipation on chip occurs in charging and discharging the video line and the column line capacitance, and the horizontal shift register clock signal. Since all three of these long wires are switched at pixel rates, they dominate all other power requirements.

3.2 LC Materials and Drive Schemes

The drive scheme in LCOS displays is determined mostly by the optical switching material requirements. There are two broad categories of these materials: bistable materials that are either fully dark or fully bright, and continuous materials that can result in partial transmittance controlled by a continuously varied voltage.

3.2.1 Bistable Materials

To produce grayscale images using bistable materials, duty-cycle modulation techniques are used. The frame time is divided into several subframes of increasing duration, one for each bit in the pixel precision. For example, to display a 3-bit pixel with an intensity of 6 (binary 110) the LC would be driven to full brightness for half a second, again to full brightness for a quarter of a second, and kept off for the final eighth of a second. The average intensity would be 6.

This drive scheme requires that each frame be redrawn B times, where B is the pixel bit precision. In each update, the full switching voltage, typically 5 volts, must be applied to each pixel, and therefore distributed to each column. Although the clock power consumption can be somewhat reduced by a parallel drive scheme, the video power consumption is substantial, since the number of image updates increases linearly with bit precision and since the materials require a full 5 V swing.

Bistable materials are typically much faster, on the order of fractions of a millisecond, which is a necessity, considering that a field-sequential bistable display of 8 bits of accuracy must wait for the LC to transition 24 times in each frame.

3.2.2 Continuous Materials

Grayscale images are simpler to produce using these materials, since gray levels can be obtained by applying an analog voltage to a pixel. The driving scheme is correspondingly similar, and consists essentially of the same task as writing to an analog DRAM cell.

There are hybrid techniques, such as digital steering of external analog voltages, in which each pixel stores a digital value that selects between a small number of video wires that carry unvarying analog voltages.

3.3 Alternate LCOS Architectures

Modifying the architecture to address several pixels in parallel can reduce the external drive circuitry speed requirements as well as internal power dissipation. There are two classes of parallel addressing: interleaved and multibanked.

In an interleaved drive scheme, several adjacent column wires are loaded in parallel, as controlled by a single shift register. The number of shift registers, and therefore the clock wire loading, is reduced, but each paralleled video wire must be distributed across the entire chip. This scheme is also compatible with a raster-based incoming data stream.

In a multibank drive scheme, the display is effectively divided into several adjacent subdisplays. Clock power due to wire capacitance is decreased compared to a serial scheme, but it is now possible to distribute each parallel video wire to only a fraction of the display, reducing video line power by the parallelization factor.

The downside of this scheme is that it cannot be used immediately with a serial data source, since the display requires multiple non-adjacent pixels at once. A video line buffer must be added to the system, increasing complexity and power requirements.

3.4 Image Property Effects on Power

The video power consumption described in the previous section assumed a worst case condition in which each pixel differs maximally from the previous one. Real images have much more correlation between adjacent pixels than this pessimistic assumption. The effect of correlated images is to reduce the power consumption due to capacitive charging, since successive pixels at the same brightness (and therefore voltage) affect only the pixel voltage and not the video and column path to the pixel, which are orders of magnitude more capacitive. Since columns function as sample-and-hold circuits, retaining the previous line's voltages, horizontal correlation decreases consumption in the video wire, while vertical correlation decreases power in the column wire. In a typical display backplane design, the column wires are more space-constrained than the video wire and are therefore more resistive and less capacitive. More precisely, capacitance ratios frequently exceed 5:1, leading to a preference for horizontal correlation.

3.5 Inversion Methods and Correlation

An additional wrinkle arises because LC materials must be driven with a zero DC field to prevent ionized contaminants from diffusing through the LC material and adhering to the pixel electrode, thus nullifying its operation. Since LC responds to the RMS voltage rather than the polarity the AC drive can be done by painting the image once with one polarity of intensity compared to the glass voltage, and then painting the same image again using the other polarity. This ideal drive method is often approximated by painting successive frames in inversion modes.

The inversion methods can occur on a frame basis, but also on a pixel-by-pixel basis, or more commonly in a row-inversion or column-inversion basis. In a row-inversion mode, alternating rows are painted in alternating polarities. Inversion drive methods aside from frame-inversion destroy image correlation in a distinctive way. Using row-inversion guarantees worst case power consumption for vertically correlated images, much as column-inversion does for horizontally correlated images. Since video wire constancy is preferred, row inversion is a more power efficient driving scheme.

Bistable material driving schemes tend to destroy correlation in images. Although the most significant bits are highly correlated, the least significant bit images are very likely to be uncorrelated. Worst-case video power consumption will likely be achieved in this case.

3.6 Color Display Issues

There are two methods used to obtain color on LCOS displays. The first method uses grayscale displays and colored light sources to achieve color. The resulting color images are combined either spatially, by using three displays and a beam splitter, or temporally, by successively illuminating a grayscale display with different colors. The latter method is called field-sequential color, and is the most common color generation method today.

The other method is spatial color, in which each pixel consists of a set of colored triads. This color is achieved either by gel filters, as with larger flat-panel displays, or with diffractive structures.

The power implications of spatial light are fairly significant. First, a field-sequential color drive scheme decreases the correlation in an image. Second, while in both spatial and temporal cases the same number of pixels must be updated per frame, (and therefore the same video power must be expended, to a first order) the clock power is reduced since three pixel values are loaded for every clock transition.

Far more significantly, the clock and video circuitry can operate much slower in the spatial color case, and therefore save power by not requiring a high-speed design. The reduced speed requirement occurs because the liquid crystal transition dead time must be expended only once per frame rather than three times per frame. To see the significance of this, consider a display operating at 60 Hz, whose LC requires 3 milliseconds to change state. The 16.6 ms frame time contains three 5.5 millisecond field times, each of which contains 3 milliseconds of dead time, and allows only 2.5 milliseconds to update the display. The effective pixel dot clock for an XGA (1024 by 768) image is 3.25 ns.

Compare this to the spatial color case, in which one field is one frame, and the live time is 13.6 milliseconds, allowing a 17.4 ns pixel period, or an improvement by a factor of five. Although the speed requirement of the FSC case can be satisfied by increasing the pixel parallelism, such an increase places a heavy burden on the drive circuitry.

4. DRIVE CIRCUITRY POWER

Until drive circuitry is integrated onto a chip, most of the display power consumption is likely to occur in the external drive circuitry. For instance, a field-programmable gate array used to control the display timing could easily consume 300 mW, over 20 times the power consumption of the display itself. Any meaningful drive circuitry analysis must therefore assume on-chip integration, or at the very least a special-purpose driver chip.

This type of analysis rapidly becomes application-specific. For example, if the video signal arrives in a standard serial analog form, such as NTSC video, a bistable material display requires an analog-to-digital converter, digital memory to store the data, a circuit to extract the intensity bits, and a digital-to-analog converter on the output. All of this circuitry dwarfs the display power consumption by two orders of magnitude.

In another critical near-term application, data arriving over a wireless digital link (such as a cellular phone) must be stored in a digital format. As a result, bit extraction and color field reordering is considerably simpler, and requires no additional circuitry. The power and cost distinctions between bistable and continuous materials become more difficult to evaluate. For example, in a bistable system, the number of memory accesses increases by the number of bit planes, but the width of each operation decreases similarly, so that the memory bandwidth and access power is the same.

5. CONCLUSIONS

Miniature information display systems are a critical component in the upcoming personal information revolution. Their design poses interesting research challenges that involve optimization across the disparate dimensions of material properties, application requirements, data representation, circuit design, and physical layout.