Separation and Extraction of Short-Circuit Power Consumption in Digital CMOS VLSI Circuits

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1. ABSTRACT

In this paper, we present a new technique which indirectly separates and extracts the total short-circuit power consumption of digital CMOS circuits. We avoid a direct encounter with the complex behavior of the short-circuit currents. Instead, we separate the dynamic power consumption from the total power and extract the total short-circuit power.

The technique is based on two facts: first, the short-circuit power consumption disappears at a V_{dd} close to V_T and, secondly, the total capacitance depends on supply voltage in a sufficiently weak way in standard CMOS circuits. Hence, the total effective capacitance can be estimated at a low V_{dd}.

To avoid reducing V_{dd} below the specified forbidden level, a polynomial is used to estimate the power versus supply voltage down to V_T based on a small voltage sweep over the allowed supply voltage levels. The result shows good accuracy for the short-circuit current ranges of interest.

1.1 Keywords

Short-circuit current, Power consumption, Power estimation.

2. INTRODUCTION

In contrast to the dominating dynamic power consumption, the short-circuit power consumption has been viewed as a power contribution of little impact in standard digital CMOS circuits. It is generally believed that the short-circuit power consumption is about 10-20% of the total power consumption [1]. Our experimental observations show that the above assumption is true for a "well-designed" circuit. However, since the short-circuit power has a linear relationship with the input transition times (Fig. 1), it can easily increase to unacceptable levels if the input signals edges are not sharp enough.

Today's VLSI circuits are complex and contain a large number of transistors. At the transistor and layout level, simulation tools usually are accurate but consume much time. Simulating the short-circuit current of even a relatively small circuit with SPICE-like programs is a very time-consuming task as the power meters in each single branch from V_{dd} and V_{ss} should measure the power at a correct time.

As the short-circuit power has been expected to be a relatively small portion of the total power consumption and as there exist no fast and reasonably accurate estimation techniques, designers are often prone to not consider the short-circuit power consumption directly. Consequently, the designer will probably not uncover the portion of the short-circuit currents which can be avoided by modifications to the design.

Several papers on the estimation of short-circuit power consumption have been published [1, 2, 3, 4]. These are quite theoretical as they give an understanding of the behavior of short-circuit currents, with various depths, depending on transistor models and approximations in the derived analytical formulas. However, the analyses and results do not extend to more than one inverter or a simple gate, and the models do not consider the signal transition dependency of multi-input gates.

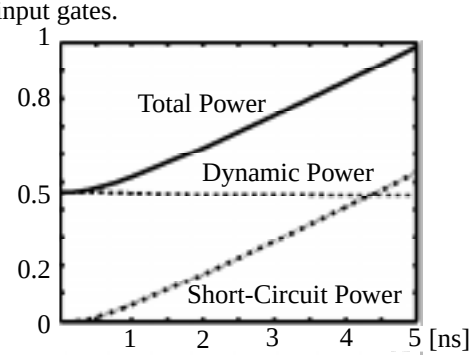

Figure 1. HSPICE simulation result of the total, dynamic and short-circuit power consumption as a function of input transition time, for an inverter loaded with another inverter (tapering factor=3).

In this paper, we present a new technique which indirectly separates and extracts the total short-circuit power consumption of a digital CMOS circuit. In Sec. 3 we present the estimation technique. We show the results in Sec. 4, and the paper is concluded in Sec. 5.

3. A NEW ESTIMATION TECHNIQUE

As was mentioned in Sec. 2, the published analytical formulas for short-circuit power consumption, P_{sc}, are all different, and depend on transistor models and approximations. However, some basic conclusions are common in most of them:

1. P_{sc} is negligible at a V_{dd} close to V_T. From a V_{dd} of about $2V_T$ and above, one transistor is always in the subthreshold region during a transition.
2. P_{sc} depends strongly on V_{dd}.
3. P_{sc} has a linear relationship with input rise or fall times. In addition, the output load also has a large impact on the short-circuit currents.

From our observations and the result of previous papers, we can conclude that the short-circuit power consumption for a general CMOS digital gate (neglecting the temperature) is a function of p- and n-MOS threshold voltages, supply voltage, transistor size, input transition time (τ), output load, and the probability of the output to toggle from a high to low or low to high voltage level, i.e.

$$P_{sc} = P_{sc}\,(\beta_n, \beta_p, V_{Tn}, V_{Tp}, V_{dd}, \tau, C_L, T, \alpha),$$

where α is the output activity factor, $\beta_n = \frac{\mu_n \varepsilon}{t_{ox}}\left(\frac{W_n}{L_n}\right)$ and T is the clock period. In a fixed design the above parameters are fixed except their possible dependency on V_{dd}.

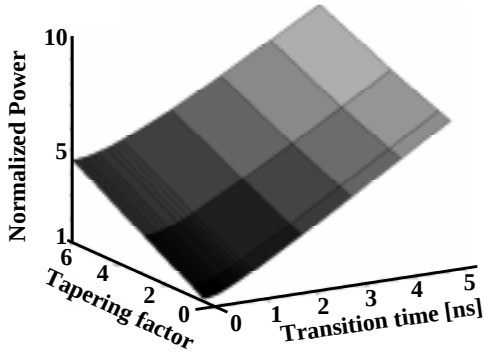

Figure 2. HSPICE simulation of the total power consumption of an inverter as a function of input transition time, loaded with another inverter with different sizes (tapering factor).

The voltage dependency of short-circuit currents is directly related to the voltage dependency of currents in a MOS transistor. This dependency changes as transistors are scaled down (short-channel effects). Let us assume that the supply voltage dependency for P_{sc} is unknown, but that it can be expressed with a polynomial function. For a single gate (i) it can be written as

$$P_{sc(i)} = \alpha_i \cdot f \cdot \Omega_i(V_{dd}),$$

where $\Omega_i(V_{dd})$ is

$$A_{i(n)} \cdot V_{dd}^{\,n} + A_{i(n-1)} \cdot V_{dd}^{\,n-1} + \ldots + A_{i(0)} \cdot$$

P_{sc} for a circuit with N gates can now be formulated as

$$P_{sc} = \sum_{1}^{N} \alpha_i \; f \; \Omega_i(V) = \alpha \; f \; \Psi(V_{dd}),$$

where $\Psi(V_{dd})$ is again a polynomial function of V_{dd} with an unknown order. The total power consumption thus is

$$P_{TOT} = P_{static} + \alpha \; f \; C \; V_{dd}^{\,2} + \alpha \; f \; \Psi(V_{dd})$$

Note that the total power can also be expressed as a polynomial function of V_{dd}. The short-circuit power consumption at V_{dd} close to V_T is negligible. Hence, for V_{dd} close to V_T, we have

$$C \cdot \alpha \cdot f = \frac{P_{TOT} - P_{static}}{V_{dd}^{\,2}}$$

The clock frequency f, V_{dd}, and the total power consumption are known. The total dynamic power consumption and, consequently, the total short-circuit power consumption for any supply voltage are readily found under following conditions:

1. The static power is negligible or known.
2. The capacitance is not unacceptably dependent on supply voltage or its dependency is known.
3. The functionality of the circuit is stable, i.e. the circuit has the same function at any supply voltage, and under full voltage swing.
4. The main input stimuli is fixed at all supply voltages.

The last condition is fulfilled if we don't intentionally change the test pattern. Condition 3 can to some extent be fulfilled by choosing a low clock frequency, but in general, we can not guarantee that any circuit will work under a wide range of supply voltage. The capacitance dependency on voltage should also be considered. In the following we discuss conditions 1-3.

3.1 Static Power Dissipation

In digital CMOS circuits, static currents are often equivalent to the (relatively) negligible leakage currents. The leakage currents are increasing in magnitude as transistor dimensions and threshold voltages are scaled down. However, they will still be relatively small as stand-by currents must be kept low.

Analog circuits in a mixed analog digital design will continuously consume power. Although standard CMOS digital circuits are the main target for the presented estimation technique, with some modifications the technique can be used also in mixed analog digital designs. Analog circuits are normally separated from the CMOS digital part (except A & D interfaces) by using separate power lines (this is today a convenient way to reduce noise). In addition, these circuits can easily be located and their power consumption (mainly the power dissipation at quiescent points) can be estimated and added to the static power consumption.

3.2 Capacitance vs V_{dd}

The capacitance of a CMOS circuit can be expressed as

$$C_{tot} = C_{MOS} + C_{int} + C_{passive} + C_{diode} \quad .$$

The interconnection capacitance and the other possible passive capacitances are not supply voltage dependent.
We divide the MOS capacitances into two major parts:

1. The capacitances that are dependent on the gate oxide thickness.
2. The diffusion capacitance (drain/source-to-bulk diode capacitances).

The gate-to-source, gate-to-drain and gate-to-bulk capacitances belong to the first part. The behavior of MOS capacitances [5] is quite complicated and a detailed analysis (in a transition) when both V_{gs} and V_{ds} are varying is beyond the scope of this paper. Still, it should be pointed out that a reduction in supply voltage is a global reduction. Similar to a higher supply voltage, transistors will operate in different operation regions (cut-off, linear and saturation) and as long as they do not continuously enter weak inversion ($V_{dd} > V_T$) the storage capacitances will not change markedly (from power consumption point of view).

The weak V_{dd} dependency on the gate capacitances can be discussed by the Mayer's capacitance model [6] which has been used over the years in simulators such as SPICE. The model is simple and quite physical. This model has several shortcomings, especially for description of short-channel devices [7,8]. However, for average capacitance estimation, the model is fully sufficient. According to this model the gate-to-source and gate-to-drain capacitances in saturation and triode regions can be expressed as:

$$\text{Saturation } V_{gs}\text{-}V_T < V_{ds} \quad \begin{pmatrix} C_{gs} = C_{gso}W + \frac{2}{3}C_o WL \\ C_{gd} = C_{gdo}W \end{pmatrix}$$

$$\text{Triode } V_{gs}\text{-}V_T > V_{ds} \quad \begin{pmatrix} C_{gs} = C_{gso}W + \frac{2}{3}C_o WL\frac{\left(3V_{sat}^2 - 2V_{ds}V_{sat}\right)}{\left(2V_{sat} - V_{ds}\right)^2} \\ C_{gd} = C_{gdo}W + \frac{2}{3}C_o WL\frac{\left(3V_{sat}^2 - 2V_{ds}V_{sat} - V_{ds}^2\right)}{\left(2V_{sat} - V_{ds}\right)^2} \end{pmatrix}$$

Where $V_{sat}=V_{gs}-V_T$ and C_o is the oxide capacitance per unit area. As is seen, in the saturation region the gate-to-source and gate-to-drain capacitances are independent of supply voltage.

In triode region, the weak supply voltage dependency of the gate capacitances can be seen by taking the $V_{gs}=V_{dd}$ and a $V_{ds} \sim 0$ (deep triode region). As long as the transistors enter into the triode region ($V_{dd} > V_T$), the amount of the capacitances are almost unchanged. Additionally, the voltage independent overlap capacitances C_{gso} and C_{gdo} take a considerable amount of the gate capacitances for minimum size devices.

The HSPICE simulation of the average variation of the gate capacitance of an inverter (Fig. 3) versus supply voltage, does not show more than about 10% in worst case. The larger part of the variation occurs at voltages close to V_T. Different capacitance models in HSPICE show somewhat different behavior. However, the above conclusions can be more or less made in all of them.

On the other hand, diodes show stronger supply voltage dependency (20-30%). Fortunately, the total MOS-diode capacitance of a standard CMOS circuit is a small fraction of the total capacitance. In addition, as supply voltage decreases, the gate capacitance decreases while MOS-diode capacitance increases, and this leads also to a smaller variation of the total capacitance with respect to V_{dd}.

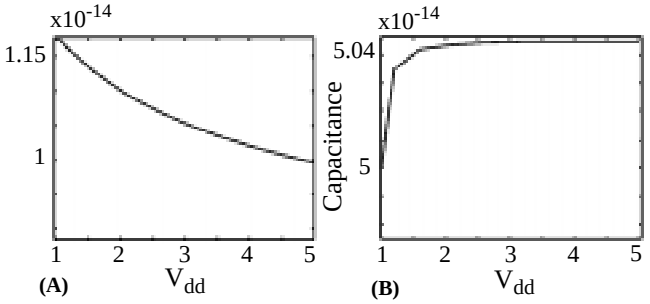

Figure 3. HSPICE simulation result of (A) the source/drain-to-bulk diffusion capacitance (MOS diodes), and (B) MOS gate capacitance versus V_{dd} (Level 47).

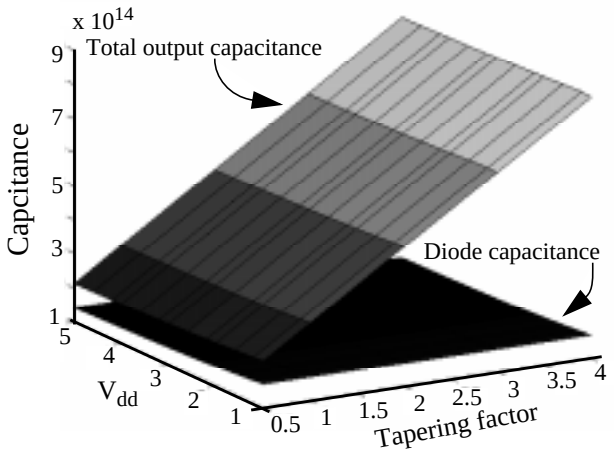

Figure 4. HSPICE simulation result of the total capacitive load at the output of an inverter (including the MOS diodes) versus V_{dd} and the tapering factor of the next inverter.

In Fig. 4 we show the average total output capacitance of an inverter, whose output is connected to another inverter with different tapering factors (MOS diode capacitance and the gate capacitance of the next stage). The ratio of diode and gate capacitance changes, since the size of the diodes are fixed whereas the gate capacitance of the next stage increases by a certain factor. This provides a realistic means for simulating the voltage dependency of the capacitances in standard CMOS circuits.

The above figures and discussion show that the total capacitance is weakly dependent on V_{dd}, and can therefore be assumed as a fixed capacitance with respect to V_{dd} .

3.3 Prediction of Total Power

We have to avoid decreasing the supply voltage below the allowable levels. Although the dependency of the total power consumption on supply voltage is quite complicated, from a mathematical point of view it presents a smooth and continuingly increasing function of supply voltage. Hence, there should exist a polynomial that can be fitted to the measured total power as a function of supply voltage. The fitting polynomial should not only give a good fit to the measured values under the known supply voltage levels but also to those that are not measured.

Among many different polynomials with different orders, the following simple polynomial shows the best global fit to all ordinary circuits in our test:

$$P_{TOT}(V_{dd}) = X_1 V_{dd}^{\ 3} + X_2 V_{dd}^{\ 2}$$

This polynomial shows physical relevance to what it describes. It has a power-2 dependency because at least the dynamic power has such a dependency.

The power-3 dependency is also expected, as the transistor currents show a power-2 dependency, so that the power consumption (= *I V*) should present a voltage dependency around a power-3. Finally, if the voltage reduces to zero then the power consumption is equal to zero.

Note that we only have to find two coefficients. Theoretically, we need only two measurements under different supply voltages. However, in practice we need more measurements in order to reduce the impact of measurement errors and noise (more measurements closer to V_T yield a better result).

On average, in Sec. 4 we did not need to reduce the supply voltage to more than 4 V from the nominal supply voltage 5 V (threshold voltage about 0.9 V). The fitting was done by the simple linear least square method.

3.4 Complete Description of the Technique

In this section we describe the technique by an example. Assume a fixed clock frequency and a voltage independent input test pattern. Suppose that we reduce the supply voltage from its nominal value with one volt (0.1 V in each step) and measure the total power consumption in each step. We put the measured values in a column vector (*B*) with 10 elements in this example.

Then we have the following equation:

$AX = B$, or

$$\begin{bmatrix} V_1^{\ 3} & V_1^{\ 2} \\ V_2^{\ 3} & V_2^{\ 2} \\ \cdots & \cdots \\ \cdots & \cdots \\ V_{10}^{\ 3} & V_{10}^{\ 2} \end{bmatrix} \bullet \begin{bmatrix} X_1 \\ X_2 \end{bmatrix} = \begin{bmatrix} B_1 \\ B_2 \\ \cdots \\ \cdots \\ B_{10} \end{bmatrix}$$

where X_i is the coefficient of the fitting polynomial to be solved.

The final solution is found by solving a set of two linear equations resulting from the least square method,

$$A^T AX = A^T B.$$

Now we can estimate the total power consumption for any supply voltage level. We choose a supply voltage equal to the threshold voltage and obtain the total power consumption at this voltage. The total dynamic power and the total short-circuit power at any supply voltage can be estimated as

$$P_{dyn}(V_{dd}) = \frac{P_{TOT}(V_T) - P_{static}}{V_T^{\ 2}} \cdot V_{dd}^{\ 2}$$

and

$$P_{sc} = P_{TOT}(V_{dd}) - P_{dyn}(V_{dd}) - P_{static}.$$

Note that the estimation technique is independent of the transistor model and explicitly independent of the process parameters and the structure of the design. It is also independent of the fitting polynomial.

Any other polynomial which gives a good global fit, can be used. However, we have chosen the used polynomial carefully. In our test, an unacceptable bad fit was always an indication of a change in functionality of the circuit and that the applied supply voltage belongs to a forbidden voltage interval.

4. SIMULATION RESULTS

The presented technique has been tested and compared with HSPICE circuit simulation result. In order to have an accurate reference simulation, the netlists of the circuits in the test bench were extracted from layout, and the contribution from drain/source-to-bulk capacitances (MOS diode capacitances) to the dynamic power consumption was carefully analyzed and taken into account.

Circuit and the number of transistors	**average (%)** $\frac{P_{dyn} - P_{sc}}{\tilde{P}_{dyn} - \tilde{P}_{sc}}$
Different drivers	7%
2 and 3-input NAND trees	8%
static XORs with different sizes	8%
static full adder, 28	11%
static 8x8 multiplier, 1840	8%
dynamic 8x8 multiplier, 3076	12%

Table 1: The result of the estimation technique $(\tilde{X})$, compared to the HSPICE circuit simulation result. P_{sc} and P_{dyn} are the average total and average short-circuit power consumption respectively. The error are measured around the nominal V_{dd} (4-5V**)**

The difference between the dynamic and the short-circuit power consumption has been used for relative error measurement. Table 1 and Fig. 5 show the estimation result of some of the different circuits with different logic styles used in the test simulations. The average errors are measured around the nominal supply voltage level (4-5V).

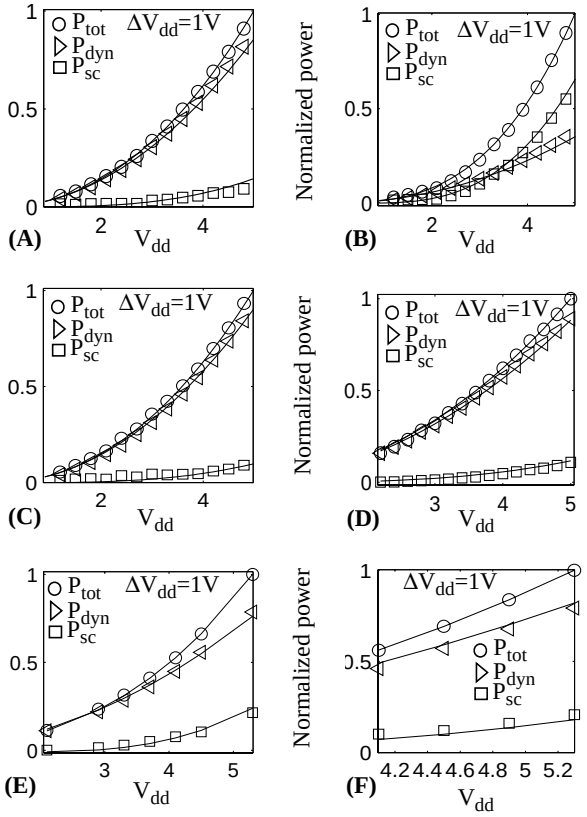

Figure 5. Comparison of the average total (P_{tot}), dynamic (P_{dyn}), and short-circuit (P_{sc}) power consumption between the result of HSPICE circuit simulation and the new estimation technique (solid line). (A) An inverter in the middle of a chain in a clock driver with tapering factor =3. (B) The inverter in the last stage of a driver with zero output load (except the intrinsic output capacitances). (C) A 3-input NAND with load. (D) A static full adder. (E) A dynamic 8x8 multiplier. (F) A static 8x8 multiplier. ΔV_{dd} is the amount of the voltage reduction needed to fit the polynomial to the total power consumption as a function of V_{dd} from the maximum level to the V_T.

Fig. 5 suggests that an overestimation of the worst case average error could, conservatively, be about 15%. Also, Fig. 5 shows that the proposed polynomial is capable of giving a good fit to the total power consumption over a sufficiently wide range of V_{dd}. The figure also shows the reason why we chose the presented error measure. Absolute and relative errors in the short-circuit power consumption alone, do not influence our judgment about how dominating the short-circuit power is.

5. CONCLUSION

We have presented a new and efficient technique for separation and extraction of the total average short-circuit and dynamic power consumption of the CMOS digital circuits. The estimation results show good accuracy for the supply voltages at which the short-circuit power consumption is not negligible. The technique does not depend on transistor models. Furthermore, the technique lends itself to chip measurements, where the dynamic and the short-circuit power fractions can be distinguished directly from measurements on the total power consumption only.

6. ACKNOWLEDGEMENT

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