On the Optimum Design of Regulated Cascode Operational Transconductance Amplifiers *

Thomas Burger and Qiuting Huang

Swiss Federal Institute of Technology, Integrated Systems Laboratory
CH-8092 Zürich, Switzerland

burger@iis.ee.ethz.ch

Abstract

An optimal design procedure to achieve minimum power consumption for a given technology and gain bandwidth is presented. Regulated cascode gain enhancement is used to ensure sufficient DC-gain at minimum gate length transistors. To validate the approach five folded cascode OTA's have been implemented, spanning a bias range of $1\mu A$ - $10mA$, with measured unity-gain bandwidths within 20% of the designed value. For 17 mW at 3 V, a 0.5 μm CMOS OTA achieves 630 MHz with 51° phase margin. The method has been applied in the design of a 3rd order $\Delta\Sigma$ modulator for GSM receivers. The modulator consumes 2.8 mW at 3 V and has a dynamic range of 86 dB for a 100 kHz input signal bandwidth.

1 Introduction

Operational amplifiers are a critical element in analog sampled-data circuits, such as SC filters, $\Delta\Sigma$ modulators and pipelined A/D converters. Higher and higher clock frequency requirement for these circuits translates directly to higher frequency requirement for the op-amp. A high gain bandwidth (GBW) is essential for accurate dynamic charge transfer in an SC circuit in a short sampling period, to realize high Q and precise poles, whereas the precise phase requirement of ideal integrators normally makes 80 dB DC-Gain, or more, desirable [1].

Today, a large part of sampled-data circuits are designed for use in battery operated devices like portable audio equipment or wireless transceivers. For the latter power consumption is one of the most critical measures, because the battery accounts for 20% of the overall cost, as well as substantial part of the weight and size, of a handset [2]. Power efficient design of all circuitry in portable equipment is therefore a key factor in reducing cost or extending lifetime of the battery. Since the op-amps usually dissipate most of the current in a sampled-data circuit they have the highest potential for power optimization.

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In this work, we demonstrate a systematic design approach for low power, high speed and high gain op-amps. Low power design is interpreted here in the sense of optimization, i.e. we seek to minimize the op-amp's power dissipation while maintaining high DC-gain, the required gain bandwidth, good phase margin and output swing. Related work is found in [3], which optimizes the interaction of the main-amp and a single gain enhancement stage, whereas our optimization approach concentrates on the main amplifier using amplifier-regulated gain enhancement to ensure high DC-gain.

We shall first describe how the use of the amplifier-regulated cascode technique frees the DC-gain consideration from the power optimization, before analyzing how the minimal power is achieved for a given GBW, acceptable phase margin and output swing. Folded cascode, known for it's good high frequency behaviour [4], serves as basic topology. Measurements of 5 OTA's will be used to validate the design approach. The pratical use of the method will be shown for the implementation of a switched-capacitor $\Delta\Sigma$ modulator.

2 Gain enhancement

The gain enhancement technique shown in fig. 1 employs an amplifier in a local feedback loop to increase the equivalent output resistance of the cascode structure [5]. The resulting DC-gain of the overall amplifier is then the product of the gain of a normal (folded) cascode amplifier with that of the regulating amplifier in the local loop. Since the latter gain compensates for the gain loss in the normal cascode structure when smaller channel lengths and higher currents are used, high DC-gain becomes relatively easy to achieve. Our own experience based on successful implementations using 1, 0.7 and 0.5 μm CMOS technologies [6], shows that even using minimum channel length transistors at relatively high current levels (mA's), more than 85 dB DC-gain can be easily achieved. An important impact of this observation is that DC-gain and speed considerations can be treated separately. The auxiliary amplifiers provide the necessary DC-gain, while the main op-amp can be optimized for speed at a given power or vice versa using minimum gate length transistors.

3 Power optimization

When the signal processing requirement dictates a particular GBW of the amplifier, such a bandwidth can be realized by different combinations of current consumption, phase margin (PM) and output

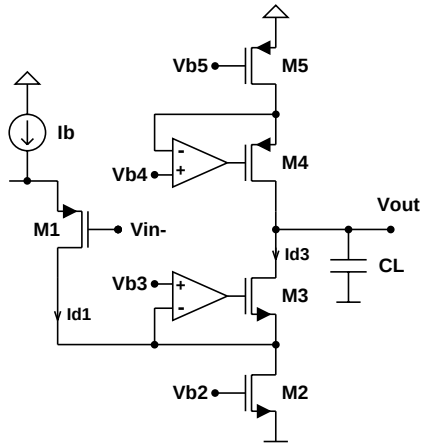

Figure 1: ***Regulated folded cascode gain enhancement***

swing (OS), which are softer system requirements that can sometimes be traded against one another within certain ranges. If we assume that high currents combined with minimum length transistors do not prevent us from achieving high DC-gain in a regulated cascode amplifier, then the design constraints for the main amp simplify to the set of equations and inequalities 1 to 5,

$$GBW = \frac{P_3}{\sqrt{2}}\sqrt{\sqrt{1+(\frac{2GBW_0}{P_3})^2}-1} \quad (1)$$

$$PM_{min} \leq 90^o - \arctan\frac{GBW}{P_3}$$

$$\rightarrow \frac{cos(PM_{min})}{sin(PM_{min})^2} \geq \frac{GBW_0}{P_3} \quad (2)$$

$$OS_{min} \leq V_{supply} - 2*(V_{dsat2}+V_{dsat3}) \quad (3)$$

$$GBW_0 = \frac{g_{m1}}{C_L + C_{db3} + C_{gd3} + C_{db4} + C_{gd4}} \quad (4)$$

$$P_3 = \frac{g_{m3}+g_{mb3}}{C_{db1}+C_{gd1}+C_{db2}+C_{gd2}+C_{gs3}+C_{sb3}} \quad (5)$$

where GBW is the unity-gain bandwidth of the OTA, GBW_0 is the gain bandwidth product and P_3 is the first nondominant pole associated with the source node of M3. The minimum acceptable phase margin and output swing (assumed symmectrical) are designated by PM_{min} and OS_{min}, respectively. Assuming minimum channel length for the critical transistors M1, M2 and M3, the design variables are thus the channel widths W_1, W_2 and W_3, plus the bias currents I_{d1} and I_{d3}, where the latter define the power consumption. In this framework minimizing power at a given gain bandwidth is equivalent to maximizing GBW for given values of I_{d1} and I_{d3} which is more convenient for mathematical treatment. Optimizing GBW means solving for the set of 5 design variables that render the highest GBW in (1), while still satisfying phase margin (2) and the output swing (3) inequalities. Maximum GBW is used here in its strict sense that assuming the process parameters used are correct, it is not possible to find a combination of transistor dimensions that yields a higher GBW for the same current.

Although analytical solutions to the above optimization can be found in special cases, in general a numerical solution is required. Many well known algorithms can be used [7]. To solve the above optimization, it is important to remember that as widths are changed while current is kept constant, the resulting transistor may either work in strong inversion, or weak and moderate inversion. Incorporating conditional checks in a numerical solver lengthens computation time and may lead to nonconvergence, so that a general model that makes continuous transition from weak to moderate and strong inversion is more expedient than piecewise formulations. In our implementation the EKV model [8] is used. The optimization is based on a 0.5 μm CMOS, N-well technology and the optimization results have been cross-checked with SPICE simulations of the obtained circuit using more sophisticated models.

Fig. 2 shows the solution space bounded by the minimum current versus GBW curve for different minimum phase margins and a given minimum output swing. I_{d1} and I_{d3} have been assumed identical to maximize slew rate, output load and supply voltage are as given in fig. 2. At low GBW's the lowest current is found with higher PM and OS than the specified minimum. As the GBW is increased the curves diverge, which signifies that the phase margin bound is held now with equality. For high GBW's the necessary minimum current increases rapidly due to the output swing constraint. At low gain bandwidth levels I_{d3} increases proportionally to GBW, showing that the input transistors are in weak inversion. As GBW increases the exponent in the I_{d3} - GBW dependence increases gradually, first to 2, signifying strong-inversion, and then towards infinity, signifying limitation by output swing.

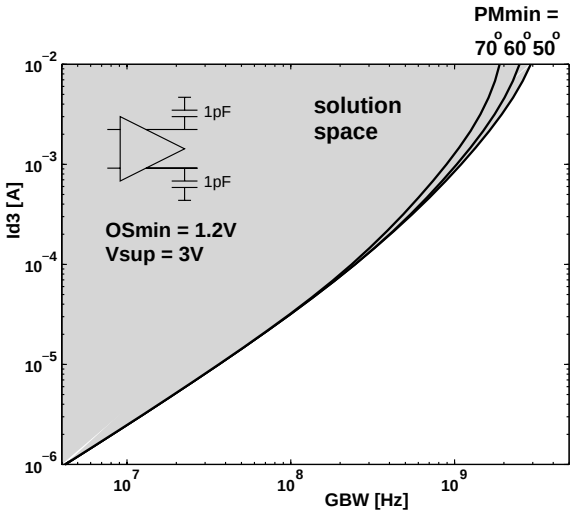

Figure 2: ***Optimal gain bandwidth vs. phase margin***

Fig. 3 shows the minimum current for a fixed minimum phase margin and different bounds on the output swing. As expected the curves of figs. 2 and 3 are identical for low levels of GBW confirming the unique GBW-I_{d3} solution at the chosen constraints on PM and OS. When GBW is increased the curves diverge and limit the achievable gain bandwidth to a region determined by the minimum output swing.

The above discussion shows that for high gain bandwidth levels, the optimum solution satisfies the equations (2) and (3) with equality. For this region phase margin and output swing can be directly traded with GBW. At lower GBW, PM and OS are not limiting the design, so that optimizing the input transistors will be the main concern to obtain minimum power dissipation while transistors M2 and M3 can be enlarged to improve matching.

In most op-amp applications a minimum output slew rate (SR_{min}) is required as well. For the OTA of fig. 1 the SR constraint is given by

$$SR_{min} \leq \frac{I_{d3}}{C_L + C_{db3} + C_{gd3} + C_{db4} + C_{gd4}} \quad (6)$$

where the expression in the denominator represents the total output node capacitance. For the high gain bandwidth region of figs. 2 and 3 the obtained slew rate is generally higher than the required minimum, since the desired gain bandwidth can only be achieved

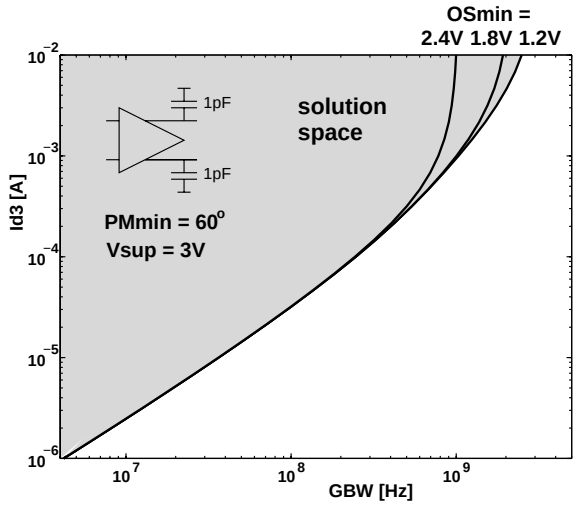

Figure 3: ***Optimal gain bandwidth vs. output swing***

with a very high current I_{d3}. In the region where I_{d3} becomes proportional to GBW an insufficient SR is more likely to result. Then (6) shifts the bound of the solution space to higher values of I_{d3}. In this situation the designer may either solve for (1) - (6) which results in suboptimum gain bandwidth or relax the slew rate requirement by reducing the node voltage swing in the application.

4 OTA implementation

To validate the optimization procedure over a wide range of bias currents and to demonstrate the kind of performance that can be achieved by it, we have implemented 5 fully differential folded cascode OTA's, each biased at ten times the current of the previous, plus a duplication of the 5th OTA, adding to it the gain enhancement. The common design parameters are: $C_L = 1\,pF, PM_{min} = 70°, OS_{min} = 1.2\,V$ (single ended). The obtained optimal transistor widths for M1 to M3 are given in table 1 together with the values for PM and OS and the maximum GBW. While the values for W1 vary less than a factor of 3 over the entire bias range, the optimum W2 and W3 differ by more than a factor of 100 due to the required output swing. The schematics of the implemented OTA's are shown in fig. 4 to 6.

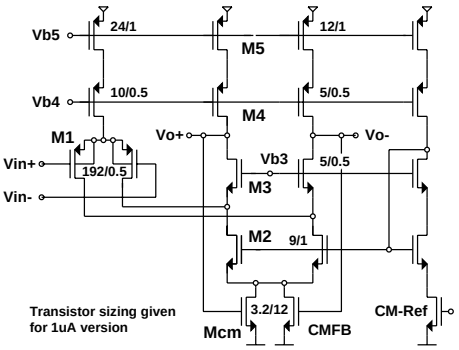

Figure 4: ***1μA and 10μA version schematic***

At low current levels the small sizes of M2 and M3 can lead to large mismatch in the bias currents and node voltages in the differential path [9]. To improve matching the widths of M2 and M3 have been enlarged and the minimum gate length strategy has been abandoned for the transistors near the rail using the reserve in PM and OS. The OTA's use a continuous-time common mode feedback, which is advantegeous for the transistor sizes used in these designs. For medium to high current levels the OTA's use dynamic common mode feedback, since the feedback transistors for a continuous time version would become impractically large for a reasonably low Vds voltage. The 1 mA and the 10 mA versions need an asymmetrical common mode range to allow for the high Vgs voltage drop of the input transistors. The regulated-cascode version of the 10 mA OTA incorporates fully differential auxiliary amplifiers with their common mode output level set at the bias voltages of the non-regulated amp. The auxiliary amps use the same dynamic common mode feedback as the main amplifier and are biased at 1/8 of the current.

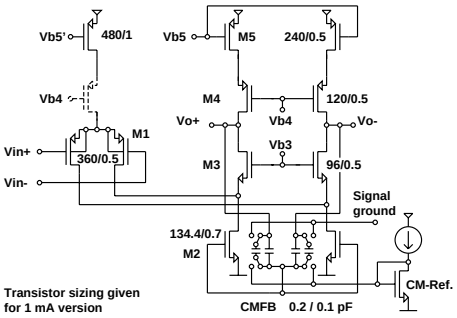

Figure 5: ***100μA to 10 mA version schematic***

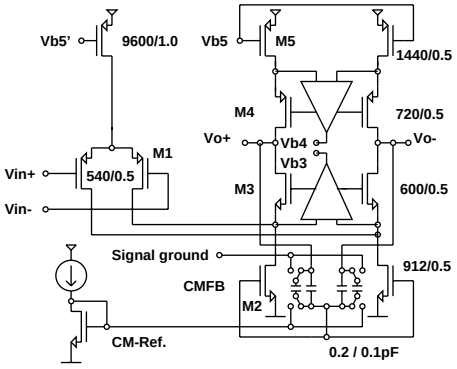

Figure 6: ***10 mA gain enhanced OTA***

5 OTA measurement

Fig. 7 shows the test setup used to measure the series of OTA's. A large output buffer stage and a feedback network with a gain of 10 have been integrated on chip to facilitate high frequency measure-

Version (I_{d3})	W1 $[\mu m]$	W2 $[\mu m]$	W3 $[\mu m]$	PM $[°]$	OS $[V]$	GBW $[MHz]$
1 μA	191.5	3.0	2.7	80.9	2.77	4.18
10 μA	299.5	5.9	10.6	74.1	2.53	36.2
100 μA	330.2	11.8	39.8	70.0	2.03	233
1 mA	351.7	44.4	96.5	70.0	1.25	887
10 mA	467.0	552.3	562.3	70.0	1.20	1880

Table 1: Optimization results

ments. Fig. 8 presents the obtained results in Bode-plot format for the case of the 1 mA OTA. The DC-gain has been measured to be 48 dB, which we know can be easily boosted to 90 dB with regulating amplifiers. The measured unity-gain frequency is 630 MHz at a phase margin of 51°.

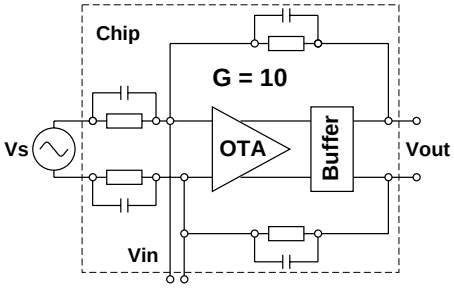

Figure 7: ***Test setup***

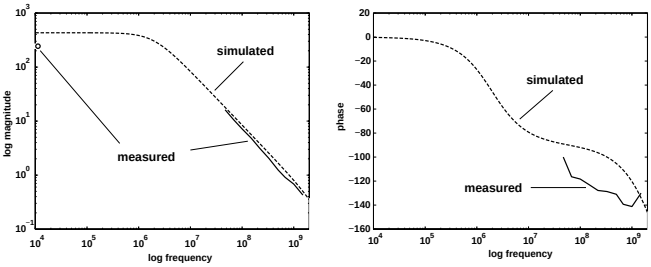

Figure 8: ***Amplitude and phase response for 1 mA OTA***

Fig. 9 shows the comparison between GBW's designed by the optimization procedure, values simulated in SPICE and those obtained by measurement. For low to medium branch current the measurements are within 20% of the designed values. Only at the 10 mA current level a large devation is observed and we are working on improving the test-setup. Table 2 summarizes the measured results of all OTA's. The output swing is given for 1 % THD, single ended. Fig. 10 shows the die photograph of the 1 mA OTA. The latter, in addition to proving the optimal design procedure, exhibits excellent performance in its own right.

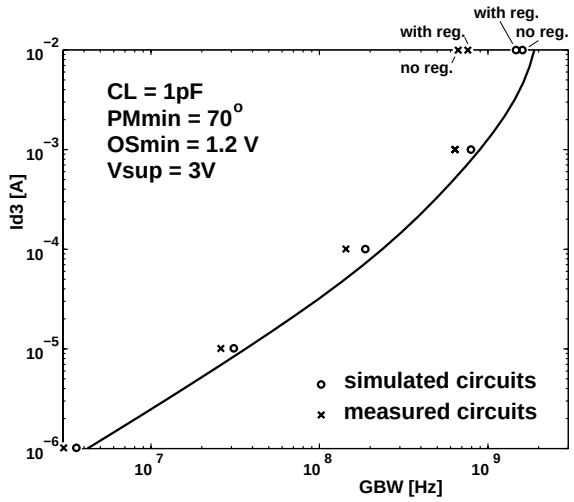

Figure 9: ***Comparison of optimization, simulation and measurement***

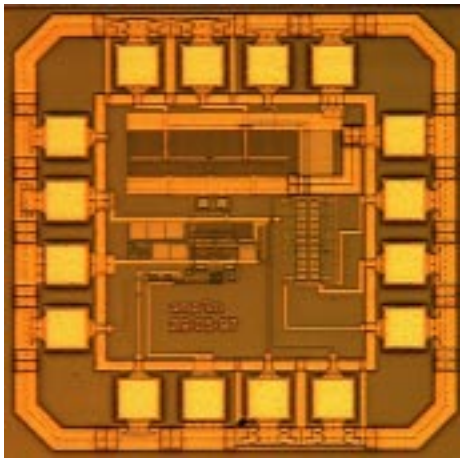

Figure 10: ***1 mA OTA chip photomicrograph***

Version (I_{d3})	DC-Gain $[dB]$	Unity GBW $[MHz]$	Phase-Margin $[deg.]$	Output Swing $[Vpp]$
1 μA	57.5	3.1	80	2.6
10 μA	63	26	64	2.55
100 μA	56	155	60	2.25
1 mA	48	630	51	1.9
10 mA (no reg.)	33	650	26	1.3
10 mA (with reg.)	66	740	21	1.3

Table 2: OTA measurement summary

6 Application example

For a mobile GSM transceiver power consumption is one of the most critical performance factors. Minimization of power in all building blocks is needed to increase stand-by and talk time, the competitive figures of merit for handsets. In the IF to baseband section of the receiver part a low power, high dynamic range A/D-converter simplifies the design of the AGC. The latter may otherwise have to be programmable over 80 dB range in 2 dB steps [10]. At 71 MHz such an AGC circuit in 0.4 μm CMOS consumes 2 mA at 3 V [11]. The baseband A/D-converter handles much lower signal frequencies and should not draw more current from the battery than the AGC. For GSM, a power budget of 5 mW should be adequate for a baseband (100 kHz) ADC with more than 80 dB of dynamic range (DR) and signal to noise and distortion ratio (SNDR).

Oversampled $\Delta\Sigma$ modulation has become the technique of choice for the baseband and voiceband signal A/D-converters in todays mobile handset because of its high dynamic range capability at low circuit complexity. Modern submicron CMOS technologies allow the clock rates for this type of converter to increase beyond 10 MHz while still maintaining a power dissipation in the order of a few milliwatts.

Fig. 11 shows a circuit diagram of the implemented 3rd order $\Delta\Sigma$ modulator, realized in fully differential SC technique. It uses a classical feedforward structure [12] with integrators, an SC summing network to the comparator and single reference feedback path to the input. The capacitance values in fig. 11 have been designed to minimize the in-band quantization noise of the modulator. The circuit adds other imperfections like switching noise, amplifier noise and harmonic distortion. To minimize the current dissipation these additional imperfections should be kept low in a power efficient manner. Due to the noise shaping property of feedback loop in $\Delta\Sigma$

modulation, errors introduced at the first stage of the circuit contribute most to such unwanted in-band distortions, whereas errors from subsequent stages are attenuated by the corresponding gain of the preceding stage [13]. The available power should therefore be used mainly for the first integrator in order to lower the amplifier originated in-band noise and to drive large capacitors in the feedback D/A-converter and the input sampler for low switching noise. We have realized a bias current ratio of 1:0.5:0.5 for the 3 OTA's, where good matching was important for the selection of capacitor sizes in the second an third integrator as well. To achieve a high power efficiency for the entire modulator we designed the power dependent in-band circuit noise at about the same level as the fixed quantization noise.

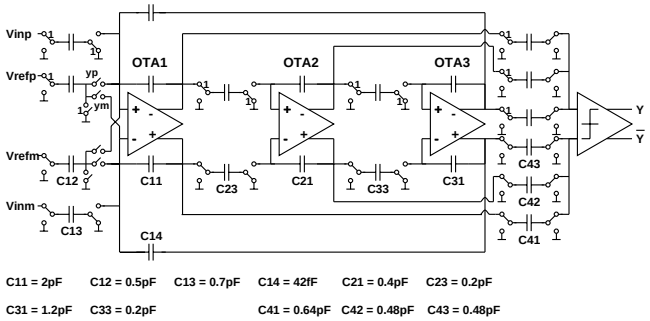

Figure 11: ***Circuit diagram of 3rd order $\Delta\Sigma$ modulator***

We have applied the analytical approach of section 3 to optimize the power in the modulator. For brevity but without losing generality we concentrate the discussion to OTA1. The capacitor values for the first integrator set the requirements for the settling behaviour parameters of OTA1. Analysis following [14] shows that slew rate $\geq$ 100 V/μs (differential) and gain bandwidth $\geq$ 56 MHz is sufficient for a peak SNDR $\geq$ 80 dB. Fig. 12 shows the basic schematic for all OTA's with numbers given for OTA1. The circuit structure is identical to the one of fig. 6. The SC common mode feedback allows us to balance the OTA's capacitive load between the two clock phases in the application.

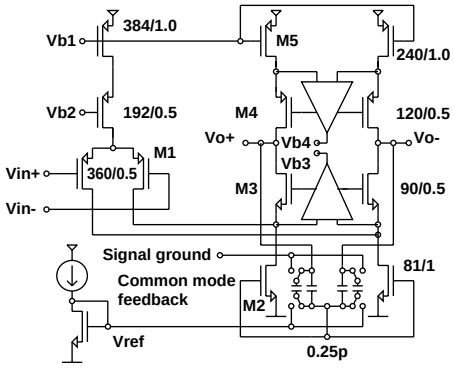

Figure 12: ***First integrator OTA schematic***

The auxiliary amplifiers of fig. 13 are biased at 1/8 of the main amplifier's current. The continuous-time common mode feedback circuit operating the MOS transistors in linear region is advantageous for the aux amps since their output swing is low when compared to the main amp so that the feedback transistors always stay in linear mode. Simultaneously they act as an output load to stabilize the amplifier. The common mode reference potentials V_{b3} and V_{b4} are determined to keep the cascode load in high-swing condition.

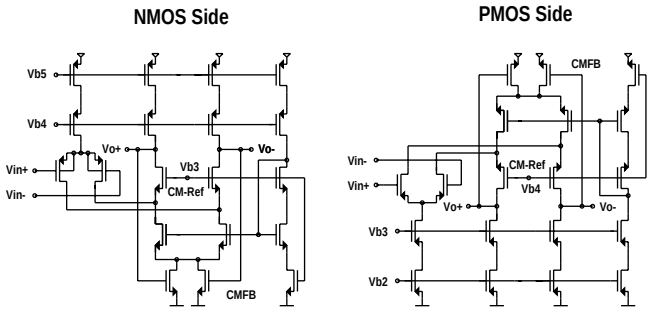

Figure 13: ***OTA1 auxiliary amplifiers***

OTA1 has been optimized in the context of the concrete circuit, i.e. for the integrating clock phase ϕ_2. For the systematic design approach (1) - (5) the load capacitance in denominator of (4) comprises therefore the effective load of the feedback network including the OTA's input capacitance. Fig. 14 gives the optimization result for the bounds PM $\geq 70^\circ$ and OS $\geq$ 2.2 V. I_{d1}=60 μA and I_{d3}=75 μA were chosen to satisfy the circuit level requirements for OTA1 leaving some reserve for the gain-bandwidth. Extra current has been given to I_{d3} to prevent cut-off of M3 and M4 and excess slewing of the aux amps. Simulated and measured GBW of OTA1 are within 30% of the optimization results. We measured a unity-gain bandwidth of 62 MHz at 75° of phase margin and a DC-gain of 101 dB. The entire circuit has a power consumption of 2.8 mW at a 3 V supply. This is far less than previously reported designs for the same application [15], [10]. Table 3 summarizes the chip characteristics.

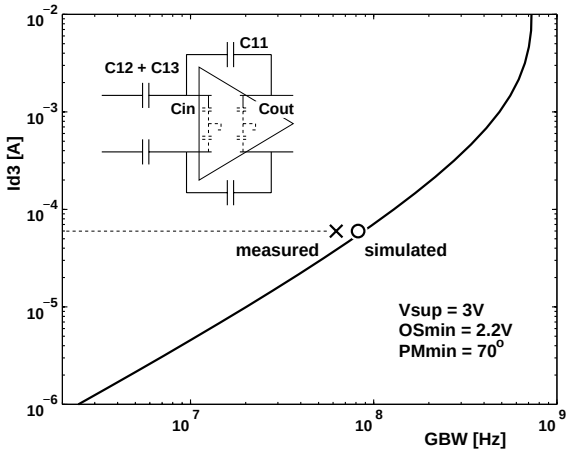

Figure 14: ***Gain bandwidth optimization of OTA1***

Diff. full scale input range	$\pm$1.2 V
Reference voltages	$\pm$1.25 V
Input sampling rate	13 MHz
Input signal bandwidth	100 kHz
Oversampling ratio	48
Dynamic range	86 dB
Peak signal to noise and dist. ratio	81 dB
Power consumption	2.8 mW
$\Delta\Sigma$ modulator chip area	0.2 mm^2

Table 3: $\Delta\Sigma$ modulator characteristics

7 Conclusions

An optimal design procedure for high performance folded cascode OTA's has been presented. It is based on an analytical formulation and minimizes power for a given technology and gain bandwidth. Regulated cascode is used to ensure sufficient DC-gain at minimum gate length transistors. Five OTA's have been implemented, spanning a bias range of $1\mu A$ - $10mA$, with measured GBW's within 20% of the designed value to validate the procedure. The practical use of the method has been demonstrated by successful implementation of a low power, 3rd order $\Delta\Sigma$ modulator for GSM applications.

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