

Voltage Scheduling Problem for Dynamically Variable Voltage Processors

Tohru ISHIHARA and Hiroto YASUURA

Department of Computer Science and Communication Engineering Graduate School of
Information Science and Electrical Engineering Kyushu University
6-1 Kasuga-koen, Kasuga-shi, Fukuoka 816-8580 Japan

E-mail: {ishihara, yasuuura}@c.csce.kyushu-u.ac.jp

Abstract

This paper presents a model of dynamically variable voltage processor and basic theorems for power-delay optimization. A static voltage scheduling problem is also proposed and formulated as an integer linear programming (ILP) problem. In the problem, we assume that a core processor can vary its supply voltage dynamically, but can use only a single voltage level at a time. For a given application program and a dynamically variable voltage processor, a voltage scheduling which minimizes energy consumption under an execution time constraint can be found.

1 Introduction

1.1 Motivation

With recent popularizations in portable, battery-powered devices such as digital cellular telephones and personal digital assistants, minimizing the power consumption of VLSI circuits becomes a more important issue.

In recent researches, datapath scheduling techniques and behavioral synthesis techniques with multiple supply voltage were proposed [2, 5, 6, 9] as the power optimization techniques. The proposed scheduling techniques refer to the assignment of a supply voltages to each operation in a data flow graph so as to minimize the average energy consumption for given computation time or throughput constraints or both. Since in such techniques, the voltage is assigned statically to each functional module, these techniques become ineffective when the time constraints vary dynamically according to the performance requirements of the applications.

In the past few years, some low power techniques by dynamic voltage scaling have been studied [3, 7, 11]. In [7], L. Nielsen et al. have shown a low-power system using self-timed circuits and adaptive scaling of the supply voltage. The self-timed circuits achieve maximum power savings by lowering the supply voltage until the chip can just meet the specific performance requirement. Their approach scales supply voltage dynamically according to the quantity of processing data per unit time. Similar to our approach, their approach can find an optimal supply voltage which is fitting to the desired performance. However, the problem definition is quite different from our approach, because their strategy to find the optimal voltage is based on adaptive methods.

Our approach is based on static scheduling technique which treats dynamically variable voltage[4].

In this paper, we propose a static voltage scheduling problem for dynamically variable voltage processors, and show guidelines to solve the problem. In addition, we formulate the problem to an ILP(Integer Linear Programming) problem. In the problem, we assume that the core processor can vary its supply voltage dynamically but can only use a single voltage at a time.

1.2 Power Delay Trade-off

The dominant source of power dissipation in a digital CMOS circuit is the dynamic power dissipation,

$$P_{dynamic} = \sum_{k=1}^M CL_k \cdot Swit_k \cdot V_{DD}^2 \quad (1)$$

where M is the number of gates in the circuits, CL_k the load capacitance of a gate g_k , $Swit_k$ the switching count of g_k per second, and V_{DD} the supply voltage. It can be said that reduction of V_{DD} is most effective for power reduction. However, reducing power supply voltage causes increase of circuit delay. The circuit delay can be estimated by the following formula,

$$\tau \propto V_{DD} / (V_G - V_T)^2 \quad (2)$$

where τ is the propagation delay of the CMOS transistor, V_T the threshold voltage, and V_G the voltage of the input gate. (1) and (2) indicate that performance must be traded for power reduction in CMOS devices. Our major contribution is to develop an effective voltage scheduling technique to optimize the power-delay trade-off.

1.3 Motivational Example

The goal of the power-delay optimization is minimizing the energy consumption by determining the voltage scheduling for a given program under a time constraint.

Let us illustrate our basic idea by a simple example. Assume that the energy consumptions of a processor are 10nJ/cycle, 25nJ/cycle and 40nJ/cycle at 2.5V, 4.0V and 5.0V, respectively. In addition, the maximum clock frequencies are 50MHz, 40MHz, and 25MHz when 5.0V, 4.0V and 2.5V are supplied, respectively. This assumptions are based on (1) and (2). Figure 1 shows three kinds of voltage schedules for the given program whose worst case execution cycles are 1000×10^6 cycles. In Figure 1(A), the total energy consumption is 40J, even if the power supply is turned off after finishing the program. Given a time constraint of 25

seconds, the voltage scheduling with 2.5V and 5.0V which fits the execution time with the given time constraint reduces the energy consumption from 40J to 32.5J. Figure 1(C) shows the ideal case of this example. If the processor uses a single supply voltage which fits the execution time just with the given time constraint, the total energy consumption is minimized. These features can be generalized by Lemma-1 and -2 in Section 2.

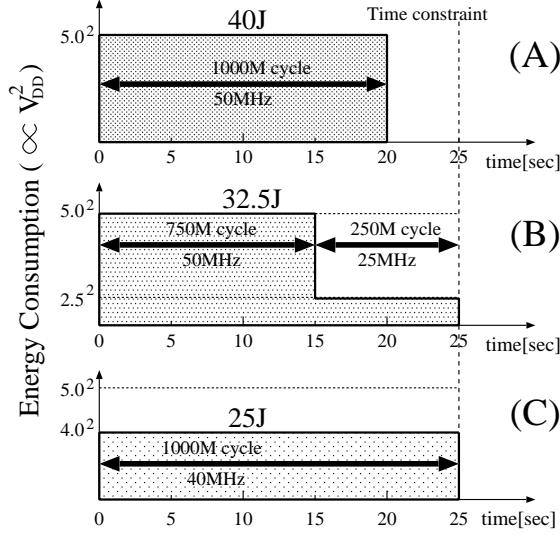


Figure 1: An example of power-delay optimization

For ideal processors which can supply continuously variable voltages, the voltage schedule (C) in Figure 1 is an optimal solution. However, using continuously variable voltages is infeasible[1], because there is some cost involved in supporting several different supply voltages[8, 10]. For a processor which has only a small number of discretely variable voltages, Theorem-1 and -2 in Section 2 can be derived as a feasible solution.

More realistic model is also discussed in Section 3. Now let us mention the new model and terms to make explanation more clearly. In Section 3, we assume the following model.

- Several tasks are executed on a processor until a specified deadline time. ($task_j$ denotes the j th task)
- For each $task_j$, EC_j : the number of execution cycles, and SC_j : average switched capacitance, are given.

The average *switched capacitance* per cycle of $task_j$ can be calculated by (3).

$$SC_j = \frac{\sum_{i=1}^{EC_j} \sum_{k=1}^M CL_k \cdot Swit_{kij}}{EC_j} \quad (3)$$

- M The number of gates in the processor.
- CL_k The load capacitance of a gate g_k .
- $Swit_{ijk}$ The switching count of g_k while the i th cycle of $task_j$ is executed.

SC_j denotes the average load for the execution of $task_j$. In processors adopting gated clock technique, SC_j will vary depending on the combination of active modules.

1.4 Paper Organization

The rest of the paper is organized in the following way. Section 2 presents basic theorems for power-delay optimization. In Section 3, a generalized theorem for realistic model which treats the *switched capacitances* of tasks are presented. In Section 4, we present ILP(Integer Linear Programming) formulation of voltage scheduling problem. Experimental results are shown in Section 5. Section 6 concludes this paper.

2 Basic Theorems on a Simple Model

In Lemma-1 and -2, we assume that processors can use continuously variable voltage between $0[V]$ and $V_{max}[V]$ (> 0). In addition, the energy consumption is assumed to be independent from the type of operations and input data, and depends only on supply voltage.

Lemma-1

If a processor completes to process a program before the deadline time T ($0 < \text{execution time} < T$), the energy consumption is not minimized.

Proof

Let us put the circuit delay $\tau(V) = \frac{k \cdot V}{(V - V_T)^\alpha}$,

then, $\frac{d\tau(V)}{dV} = -\frac{(\alpha - 1) + k \cdot V_T}{(V - V_T)^{\alpha+1}} < 0$

(k : constant! $0 < V_T < V$, $1 \leq \alpha \leq 2$)

It is immediate that the $\tau(V)$ is monotonously decrease function of voltage V as shown in Figure 2. The α strongly depends on the mobility degradation of electrons in transistors, and tends to be decreased from 2.0 to 1.0 when the channel size is scaled down. Threshold voltage V_T also tends to be decreased to improve transition delay and propagation delay of transistors. It is immediate that the energy consumption is a monotonously increase function of voltage V as shown in Figure 2. \square

This feature substantiates the well known power-delay trade-off in CMOS circuits for any practical α and V_T . A significant knowledge from Lemma-1 is that the performance must be traded for energy reduction even if the transistor size and V_T are scaled down.

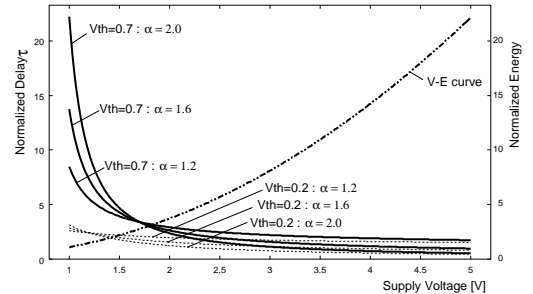


Figure 2: V- τ curve for various V_T and α

Lemma-2

If a processor uses a single supply voltage v and completes a program just at a deadline time $T(> 0)$! the v is an unique supply voltage which minimizes energy consumption for the processing.

Proof

For any v ($0 < V_T < V_1 < v < V_2 < V_{max}$) and x ($0 \leq x \leq EC$), we prove (5) under the constraint (4). Where EC stands for total execution cycles of the given program.

$$\frac{x \cdot V_1}{(V_1 - V_T)^\alpha} + \frac{(EC - x) \cdot V_2}{(V_2 - V_T)^\alpha} = \frac{EC \cdot v}{(v - V_T)^\alpha} \quad (4)$$

$$V_1^2 \cdot x + V_2^2 \cdot (EC - x) > v^2 \cdot EC \quad (5)$$

The left sides of (4) and (5) represent the total execution time and energy consumption, respectively, when x cycles are executed with voltage V_1 and $EC - x$ cycles with voltage V_2 . The right side of (4) and (5) represent total execution time and energy consumption, respectively, when all cycles are executed with voltage v .

$$\text{Put, } T = \frac{x \cdot V_1}{(V_1 - V_T)^\alpha} + \frac{(EC - x) \cdot V_2}{(V_2 - V_T)^\alpha} = \frac{EC \cdot v}{(v - V_T)^\alpha},$$

$$f = V_1^2 \cdot x + V_2^2 \cdot (EC - x), \quad \text{and} \quad g = v^2 \cdot EC$$

It can immediately be derived that f is a linear function of the deadline time T as shown in Figure 3. In addition, g is a below convex function of the deadline time T . Consequently, (6) is proved under the constraint of (4).

$$f - g < 0 \quad (6)$$

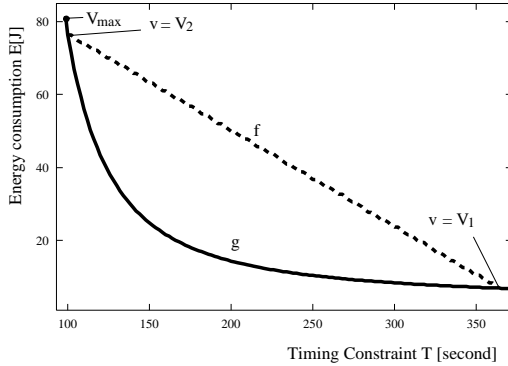


Figure 3: Energy consumption versus time constraint

(6) indicates that the voltage scheduling with two voltages can not minimize energy consumption. Furthermore, it is obvious that the voltage scheduling with more than two voltages can not minimize energy consumption. \square

We denote the ideal voltage which is mentioned in Lemma-2 as follows.

v_{ideal} : An unique supply voltage which adjusts the total execution time just to the given deadline time.

For ideal processors which can supply continuously variable voltages, processing with the v_{ideal} minimizes energy consumption. However, using continuously variable voltage is infeasible[1], because preparing any kinds of stable supply voltages and clock frequency wastes the significant power and hardware cost. In other words, processors can not always use a single specified voltage which minimizes energy consumption. For processor which have only a small number of discretely variable voltages, Theorem-1 and -2 are derived as feasible solutions.

Theorem-1

If a processor can use only a small number of discretely variable voltages, the voltage scheduling with at most two voltages minimizes the energy consumption under any time constraint.

Proof

Consider the following two kinds of voltage scheduling : *schedule-1* is the schedule with three voltages V_1 , V_2 , and V_3 ($0 < V_1 < v_{ideal} < V_2 < V_3$), and *schedule-2*, the schedule with two voltages V_1 and V_2 . Now, let the execution cycles with V_1 , V_2 , and V_3 in *schedule-1* be $x_1 (\geq 0)$, $x_2 (\geq 0)$, and $x_3 (\geq 0)$, respectively. In addition, $y_1 (\geq 0)$ and $y_2 (\geq 0)$ cycles are assumed to be executed with V_1 and V_2 in *schedule-2*, respectively. We prove (7), under the constraints of (8) and (9).

$$V_1^2 \cdot x_1 + V_2^2 \cdot x_2 + V_3^2 \cdot x_3 \geq V_1^2 \cdot y_1 + V_2^2 \cdot y_2 \quad (7)$$

$$\begin{aligned} \frac{x_1 \cdot V_1}{(V_1 - V_T)^\alpha} + \frac{x_2 \cdot V_2}{(V_2 - V_T)^\alpha} + \frac{x_3 \cdot V_3}{(V_3 - V_T)^\alpha} \\ = \frac{y_1 \cdot V_1}{(V_1 - V_T)^\alpha} + \frac{y_2 \cdot V_2}{(V_2 - V_T)^\alpha} \end{aligned} \quad (8)$$

$$x_1 + x_2 + x_3 = y_1 + y_2 \quad (9)$$

The left and right sides of (7) represents the energy consumption of *schedule-1* and *schedule-2*, respectively. (8) and (9) explain that the total execution time and the execution cycles of two schedules must be same.

First, assuming $x_1 < y_1$, it is immediate that the constraints (8) and (9) can not be satisfied. Consequently, the situation $x_1 < y_1$ can not occur. Therefore, we have only to consider the situation $x_1 \geq y_1$. In this situation, (7), (8) and (9) can be deformed as (10), (11), (12), and (13).

$$(x_1 - y_1) + x_3 = y_2 - x_2 \quad (10)$$

$$\frac{(x_1 - y_1) \cdot V_1}{(V_1 - V_T)^\alpha} + \frac{x_3 \cdot V_3}{(V_3 - V_T)^\alpha} = \frac{(y_2 - x_2) \cdot V_2}{(V_2 - V_T)^\alpha} \quad (11)$$

$$V_1^2 \cdot (x_1 - y_1) + V_3^2 \cdot x_3 \geq V_2^2 \cdot (y_2 - x_2) \quad (12)$$

$$x_1 - y_1 > 0, \quad y_2 - x_2 > 0, \quad x_3 > 0 \quad (13)$$

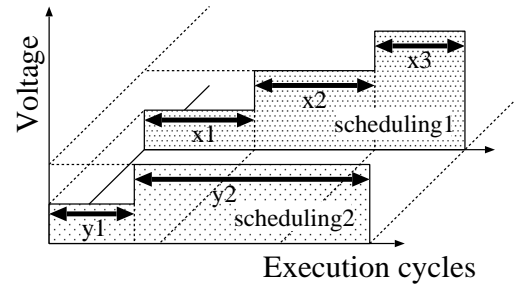


Figure 4: Voltage scheduling-1 versus scheduling-2 (2)

From Lemma-2, (12) can be immediately proved under the constraints of (10), (11), and (13). Therefore, voltage scheduling with V_1 , V_2 , and V_3 can not minimize energy consumption, when $0 < V_1 < v_{ideal} < V_2 < V_3$. Similarly,

it is easy to prove that the energy consumption of voltage scheduling with V_2 and V_3 is smaller than that with V_1 , V_2 and V_3 , when $0 < V_1 < V_2 < v_{ideal} < V_3$. Consequently, voltage scheduling with three voltage can not minimize energy consumption. The voltage scheduling with more than three voltages also can not minimize energy consumption. Theorem-1 is proved. \square

Theorem-1 and -2 indicate significant feature of voltage scheduling. That is, only one time voltage alteration can minimize the energy consumption. Therefore time and power overhead of voltage alteration can be neglected for the practical real-time constraints.

Theorem-2

If a processor can use only a small number of discretely variable voltages, the two voltages which minimize the energy consumption under a time constraint T are immediate neighbors to the voltage v_{ideal} .

Proof

Assume that the processor can use three voltages V_1 , V_2 , and V_3 . It has already been proved that the energy consumption is a linear function of the time constraint when the processor uses only two voltages as shown in Figure 5. If the time constraint T satisfies $t_3 < T < t_2$, voltage scheduling with V_3 and V_2 minimize energy consumption. In case that the time constraint T satisfies $t_2 < T < t_1$, voltage scheduling with V_2 and V_1 minimize energy consumption. Therefore, it is clear that the voltage scheduling with V_3 and V_1 can not minimize energy consumption. Consequently, the scheduling with two voltages which are immediate neighbors to the ideal voltage v_{ideal} minimizes the energy consumption. \square

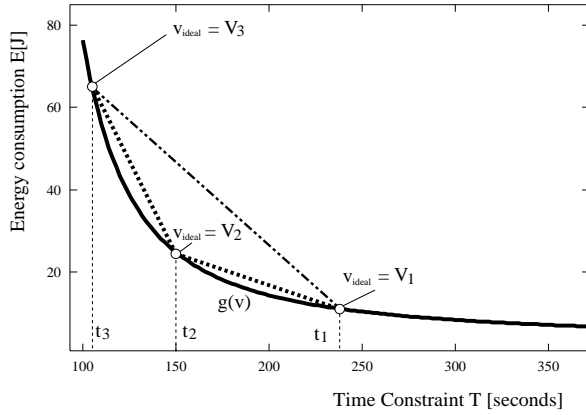


Figure 5: Voltage scheduling with two voltages

3 Generalized Theorems on a Realistic Model

If the average switched capacitances per cycle (SC_j s) are largely different, the features which are explained in Figure 1 are not always true. For a set of tasks $\{task_1, task_2\}$ as shown in Figure 6, the voltage scheduling with 2.5V and 5.0V as shown in Figure 6(E) reduces much energy compared to that with a single voltage (4.0V) as shown in Figure 6(D). A point to notice is that the total switched capacitance ($\sum EC_j \times SC_j$) of the both scheduling are same from each other. For both voltage schedules, the processor completes

the 1000M cycles of the program just at the time constraint. The x, y, and z axes of graphs (D) and (E) represent that the execution cycles, the square of supply voltage, and the SC_j respectively. The volume of cubes represents the energy consumption for processing.

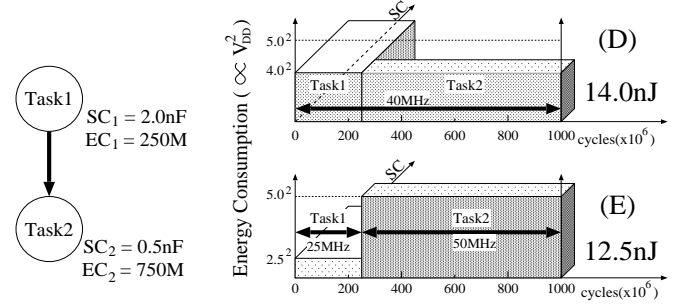


Figure 6: Voltage scheduling considering SC_j

If SC_j s can be estimated statically, much energy reduction can be expected. Establishing an accurate technique to estimate SC_j s is our future work. This feature is generalized by Lemma-3 and Theorem-3.

In the rest of this section, we targets the set of tasks whose SC_j are different from each other. If the SC_j s are different from each other, Lemma-3 and Theorem-3 can be derived.

Lemma-3

If a processor uses continuously variable voltages, the voltage scheduling which assigns a single voltage for each task minimizes energy consumption for a given program under a time constraint.

Proof

Assume that more than one voltage are scheduled to a certain task. From Lemma-2, it is obvious that this scheduling can be replaced by the scheduling with a single voltage, leaving the execution time unchanged and reducing the energy consumption for the task. \square

Theorem-3

If a processor can use only a small number of discretely variable voltages and SC_j s are different from each other, the voltage scheduling with at most two voltages for each task minimizes energy consumption for the program under a time constraint.

Proof

Similar to Proof of Theorem-1 and -2, Theorem-3 can be easily proved from Lemma-2. \square

4 ILP Formulation

4.1 Assumptions

In a simplified voltage scheduling problem, we target systems which assume the following:

- The system is a processor based hard real-time system.

- The processor can vary its supply voltage dynamically.
- The processor uses only a small number of discrete voltages.
- The processor equips an adaptive clock scheme which closely tracks the supply voltage.
- The processor can vary the supply voltage at any clock cycle.
- Time overhead to vary the supply voltage and clock frequency is negligible.
- Power loss for the DC-DC converter is negligible.
- The worst case execution cycles of the given program can be estimated statically.

4.2 Notation

The variables used in the formulation are defined as follows.

- N The number of tasks. $N = |\{task_j\}|$.
- $task_j$ The j th task. ($1 \leq j \leq N$).
 $task_j = (EC_j, SC_j)$.
- EC_j The number of execution cycles of the j th task.
- SC_j The average *switched capacitance* for the j th task.
- L The number of variable voltages of target processor. $L = |\{mode_i\}|$.
- $mode_i$ The i th execution mode of the processor.
 $mode_i = (V_i, F_i)$.
- V_i The i th voltage. ($1 \leq i \leq L$).
- F_i The clock frequency when the supply voltage is V_i . F_i is calculated by (2).
- T The time constraint until which all given tasks must be completed.
- x_{ij} The number of cycles of the task j executed with voltage V_i .

4.3 Formulation

The voltage scheduling problem is formulated as follows:

$$\text{Minimize } E = \sum_{j=1}^N \sum_{i=1}^L SC_j \cdot x_{ij} \cdot V_i^2 \quad (14)$$

$$\text{subject to } \sum_{i=1}^L x_{ij} = EC_j, \quad \sum_{j=1}^N \sum_{i=1}^L \frac{x_{ij}}{F_i} \leq T \quad (15)$$

The voltage scheduling problem is formally defined as follows.

“For given $\{task_j\}$ and $\{mode_i\}$, find x_{ij} which minimize E satisfying the time constraint T .”

5 Experimental Results

First, we show the experimental result for a set of tasks $\{task_1, task_2, task_3\}$. The average *switched capacitances* and execution cycles of these three tasks are $\{SC_1, EC_1\} = \{50pF, 50 \times 10^9\}$, $\{SC_2, EC_2\} = \{100pF, 50 \times 10^9\}$, and $\{SC_3, EC_3\} = \{150pF, 50 \times 10^9\}$. The purpose of this experiment is to clarify the relation between the variety of variable voltages and effect of energy reduction. In this example we assume seven kinds of variable voltage processor as shown in 1. We assume the processor can vary the supply voltage dynamically but can use only a single voltage at a time.

Table 1: Variation of variable supply voltages

Processors	Variable supply voltages
Processor-1	Only 3.3V
Processor-2	3.3V and 0.9V
Processor-3	3.3V and 1.7V
Processor-4	3.3V and 2.5V
Processor-5	3.3V, 2.5V and 0.9V
Processor-6	3.3V, 2.5V, 1.7V, and 0.9V
Processor-7	Any voltage between 3.3V and 0.9V

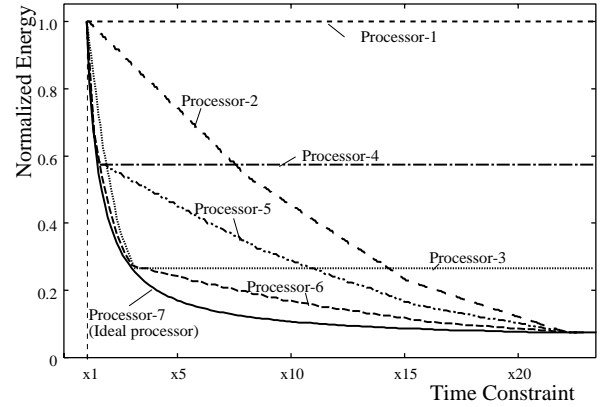


Figure 7: Variation of voltages versus energy reduction

The result in Figure 7 shows that if the number of variable voltages are increased, energy consumption can be reduced at least. Selecting suitable voltages for applications leads to drastic energy reduction even if the number of variable voltages is very small.

Next, we show the experimental result for four programs (program = $\{task_1, task_2, task_3\}$) as shown in the table 2.

Table 2: Specification of sample programs

Program	(EC_1, EC_2, EC_3)	(SC_1, SC_2, SC_3)
Program-1	$(50, 50, 50) \times 10^9$	$(100, 100, 100)[pF]$
Program-2	$(50, 50, 50) \times 10^9$	$(80, 100, 120)[pF]$
Program-3	$(50, 50, 50) \times 10^9$	$(40, 100, 160)[pF]$
Program-4	$(50, 50, 50) \times 10^9$	$(20, 40, 240)[pF]$

The numbers in the left side parentheses represent the number of the execution cycles of task1, task2, and task3 respectively, and right side parentheses represent the average *switched capacitance* of task1, task2, and task3 respectively. In addition, we use two types of processors : *processor-2* and *processor-6* which appear in Table1. The number of the

execution cycles of tasks are same from each other in this experiment. In addition, the sum of SC_j s of each program is the same. The assumption for clock frequency properly obeys (2). We assume that the V_T in (2) is 0.6V in this experiment. Experimental results are shown in Figure 8.

The experimental results show that the voltage scheduling with multiple voltages is more effective for energy reduction, if the SC_j s are more different from one task to another even if the sum of SC_j s is constant. Comparing program-1 with program-4, energy consumption of processor-2 is reduced by 70% at best case. If the SC_j s of given tasks are much different from each other, assigning lower voltage to the tasks whose SC_j s are bigger and higher voltage to the tasks whose SC_j s are smaller leads to drastic energy reduction. Of course, energy consumptions are decreased according to how the time constraint is relaxed.

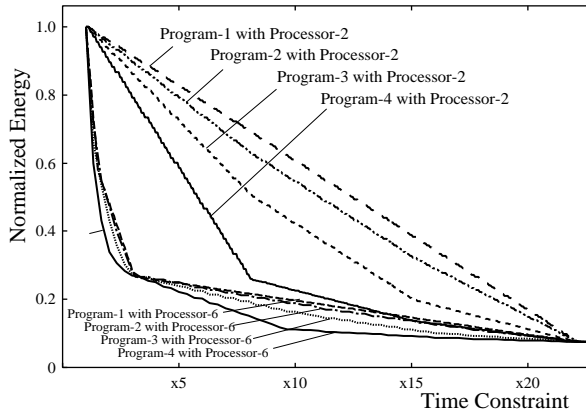


Figure 8: Variation of SC_j versus energy reduction

From the results, we have the following observations:

1. An increase of the number of variable voltages may have weak impact on energy reduction. However, selecting suitable voltages for applications leads to drastic energy reduction even if the number of variable voltages is very small.
2. Even if the time constraint is constant, assigning lower voltage to the tasks whose SC_j s are bigger and higher voltage to the tasks whose SC_j s are smaller reduces total energy consumption by 70% at maximum case. For application programs whose SC_j is widely varied by operating conditions, voltage scheduling is very effective for energy reduction.

6 Conclusion

In this paper, we present a system model which contains the dynamically variable voltage processor and present basic theorems for power-delay optimization. The static voltage scheduling problem is also proposed and formulated as an integer linear programming (ILP) problem. In the problem, we assume that the core processor can vary its supply voltage dynamically, but can use only a single voltage level at a time. Significant theorems presented in this paper are summarized below.

- Power-delay trade-offs in CMOS circuits are substantiated for any practical V_T and α (Lemma-1).
- If a processor can use consecutive voltage, only a single voltage can minimize energy consumption satisfying the time constraint (Lemma-2).
- If a processor can use only a small number of discrete voltages, the voltage scheduling with at most two voltages minimizes energy consumption under any time constraints (Theorem-1).
- Two voltages which minimize energy consumption under a time constraint are immediate neighbors to the v_{ideal} (Theorem-2).

Theorem-1 proves significant features of static voltage scheduling. That is, only one time voltage alteration can minimize the energy consumption. Therefore time and power loss for voltage alteration can be neglected if the real-time system gives a long period of deadline time compared to the time overhead to vary the supply voltage. The theorem for a set of tasks whose SC_j s are different from each other is also presented.

Our future work will be devoted to extend the proposed optimization problem considering the actual design of DC-DC level converter and task scheduling.

References

- [1] A. P. Chandrakasan and R. W. Brodersen, *LOW POWER DIGITAL CMOS DESIGN*, Kluwer Academic Publishers, 1995.
- [2] Jui-Ming Chang and Massoud Pedram, "Energy Minimization Using Multiple Supply Voltages," *IEEE Trans. VLSI Systems*, vol.5, no.4, pp.436-443, December 1997.
- [3] Vadim Gutnik and Anantha P. Chandrakasan, "Embedded Power Supply for Low-Power DSP," *IEEE Trans. VLSI Systems*, vol.5, no.4, pp.425-435, December 1997.
- [4] T. Ishihara and H. Yasuura, "Optimization of Supply Voltage Assignment for Power Reduction on Processor-Based Systems," In *Proc. of SASIMI '97*, pp.51-58, 1997.
- [5] Mark C. Johnson and Kaushik Roy, "Dathpath Scheduling with Multiple Supply Voltages and Level Converters," *ACM Trans. DAES*, vol.2, no.3, pp.227-248, July 1997.
- [6] Yann-Rue Lin, Theng-Tsung Hwang, and Allen C.-H. Wu, "Scheduling Techniques for Variable Voltage Low Power Designs," *ACM Trans. DAES*, vol.2, no.2, pp.81-97, April 1997.
- [7] Lars S. Nielsen, Cees Niessen, Jens Sparsø, and Kees van Berkel, "Low-Power Operation Using Self-Timed Circuits and Adaptive Scaling of the Supply Voltage," *IEEE Trans. on VLSI system*, vol.2, no.4, pp.391-397, December 1994.
- [8] Jan M. Rabaey and Massoud Pedram, *Low Power Design Methodologies*, Kluwer Academic Publishers, 1996.
- [9] Salil Raje and Majid Sarrafzadeh, "Variable voltage scheduling," In *Proc. of International Symposium on Low Power Design*, pp.9-14, 1995.
- [10] A. J. Stratakos and S. R. Sanders R. W. Brodersen, "High-Efficiency Low-Voltage DC-DC conversion for Portable Applications," In *Proc. of IWLPD*, pp.105-110, Apr. 1994.
- [11] Gu-Yeon Wei and Mark Horowitz, "A Low Power Switching Power Supply for Self-Clocked Systems," In *Proc. of ISLPED'96*, pp.313-317, 1996.