Low Swing Interconnect Interface Circuits

Hui Zhang
EECS Department
University of California at Berkeley
510.643.9380
hui@eecs.berkeley.edu

Jan Rabaey
EECS Department
University of California at Berkeley
510.643.8206
jan@eecs.berkeley.edu

1. ABSTRACT

This paper reviews a number of low-swing on-chip interconnect schemes, and presents a thorough analysis of their effectiveness and limitations. In addition, several new interface circuits, presenting even more energy savings, are proposed. Some of these circuits not only reduce the interconnect swing, but also use very low supply voltages, so as to obtain quadratic energy savings. The performances of each of the presented circuits are thoroughly examined using simulation on a benchmark interconnect circuit. Energy savings with a factor of seven have been observed for some of the schemes.

2. INTRODUCTION

In the deep-submicron era, interconnect wires (and the associated driver and receiver circuits) are responsible for an ever increasing fraction of the energy consumption of an integrated circuit. Most of this increase is due to global wires, such as busses and clock and timing signals. This observation is particularly true for reconfigurable circuits. For instance, it has been observed that more than 90% of the power dissipation of traditional FPGA components (over a wide range of applications) is due to the interconnect [1]. For gate array and cell library based designs, Dake Liu [8] found that the power consumption of wires and clock signals can be up to 40% and 50% of the total on-chip power consumption respectively. Obviously, techniques that can help to reduce these ratios are very desirable. Short of reducing the average length of the wires and their fanout by using advanced processes or improved architectures, reducing the voltage swing of the signal on the wire is the best bet towards getting better energy efficiency. In this paper, we will analyze the effectiveness of a number of reduced swing interconnect schemes that have been proposed in the literature [2-6]. In addition, a number of novel or modified circuits will be introduced, simulated, and critiqued. To present a fair and realistic base for comparison, a single test circuit will be used. Overall, it is found that the proposed schemes present a wide range of potential energy reductions, yet that other considerations such as complexity, reliability, and performance play important roles as well.

The paper is organized as follows. In section 3, the test bed that will be used in all simulations is presented. This is followed by a review and comparison of a number of architectures, obtained from the open literature. Several novel or modified low-swing schemes are proposed and analyzed in section 5. Finally, section 6 brings them all together and draws some conclusions.

3. TEST ARCHITECTURE AND QUALITY METRICS

Presenting a fair comparison for the various interconnect schemes that are presented in this paper requires a common and fair test-bed. Fig. 1(a) illustrates the schematic of our benchmark interconnect circuit. The driver converts a full-swing input into a reduced-swing interconnect signal, which is converted back to a full-swing output by the receiver. The interconnect line is a metal-3 layer wire with a length of 10 mm, modeled by a π3 distributed RC model with an extra capacitive load C_L distributed along the wire (for fanout), as shown in Fig. 1(b). To fairly compare the delays of different

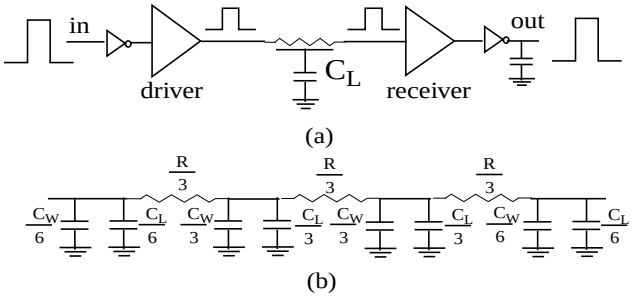

FIGURE 1. (a) Benchmark testing architecture; (b) Interconnect model.

schemes, we deliberately add an inverter prior to the driver and an inverter after the receiver with 20fF capacitive load. Both inverters are sized with Wp=6 um and Wn=3 um. All circuit comparisons are based on the MOSIS HP CMOS14TB process parameters and spice models. The minimum drawn channel length for this process is set to 0.6 um with an effective channel length of 0.5 um.

While energy minimization is the ultimate goal of our study, a range of metrics have to be considered to make the analysis meaningful.

- Energy — The dynamic energy of the interconnect is given by (EQ 1). The data switching activity is also a factor comparing schemes with different types of circuit design such as dynamic design versus static design.

$$E_{dyn} = (C_W + C_L) \cdot V_{DD}(driver) \cdot V_{swing} \quad (EQ\ 1)$$

- Area and design complexity.
- Speed.
- Reliability — Three main sources of reliability degradation have to be considered: process variation, voltage supply noise, and inter-line crosstalk. As for process variation, the most important parameters are the threshold voltage variation and mismatch of transistors. For each circuit, we consider the corner cases and perform a Monte Carlo analysis with a 10% VDD fluctuation and 10% threshold voltage variation. For the crosstalk noise due to interline coupling, we only examine the worst-case scenario: a single global line paralleled with two minimum-spaced neighboring wires.

4. REVIEW OF EXISTING LOW SWING INTERFACE CIRCUITS

In this section, seven low swing circuit schemes are reviewed, and the pro's and con's of each approach are enumerated. The first three schemes use static drivers, while the rest dynamically drive the wires. The important design metrics of the circuits are compared based on simulation results.

4.1 Static Driver With Reduced Supply

The Conventional Level Converter (CLC) showed in Fig. 2

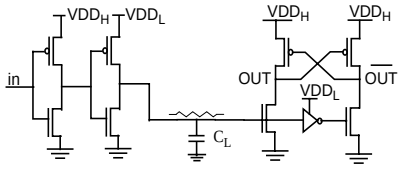

FIGURE 2. Conventional level converter

is the traditional circuit to convert a low swing signal back to a full swing one. The driver uses an extra supply with lower voltage to drive the interconnect from 0 to VDD_L. Although the noise margin is reduced, this circuit is very robust against noise, since the receiver behaves as a differential amplifier, and the internal inverter further attenuates some noise through regeneration. The Symmetric Driver and Level Converter (SDLC) scheme proposed in [2] is also a good example within this category. It needs two extra power rails to limit the interconnect swing, and uses special low Vt (~0.1V) devices to compensate the current drive loss due to the lower supplies.

4.2 DIFFerential Interconnect (DIFF)

Differential signaling has better noise immunity due to its common mode rejection, so the signal swing can be further reduced. Fig. 3 shows an example circuit proposed in [9], which produces quadratic energy savings by using a very low voltage supply. The driver uses NMOS for both pull-up and pull-down. The receiver is an unbalanced current latch sense amplifier. The receiver adds area overhead, and it

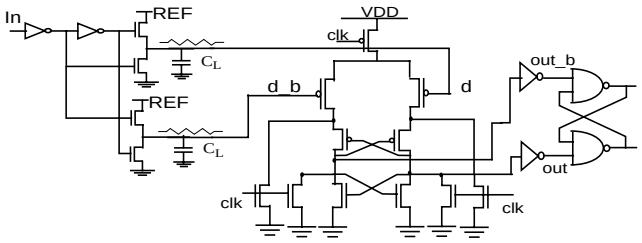

FIGURE 3. Differential low swing interconnect

consumes energy for every cycle. Therefore, for short interconnect with small capacitive load, the overhead of the receiver may become dominant. The operation of the sense amplifier is sensitive to the device mismatch between P1 and P2, but not to the supply noise. In general, one problem with differential schemes is that the number of wires is doubled, which certainly presents a major concern in most designs. Another overhead is the extra clock signal.

4.3 Dynamically Enabled Drivers

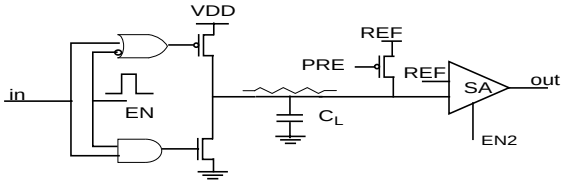

FIGURE 4. Pulse-controlled driver with sense amplifier

Within this category, the basic idea is controlling the (dis)charging time of the drivers to obtain a desirable swing on the interconnect. The Pulsed-Controlled Driver (PCD) showed in Fig. 4 is such a typical circuit. The advantage of this circuit is that the pulse width can be fine-tuned to realize a very low swing while no extra voltage supply is needed. However, it only works well if the capacitive loads are well-known beforehand. Furthermore, the floating wire when the driver is disabled is susceptible to noise. The *RSD_VST* scheme proposed in [5] also dynamically controls the driver, but with an internal control signal. The receiver, called Voltage Sense Translator (VST), converts a low-swing signal to a full-swing one. The driver uses an embedded VST to sense the interconnect swing so as to provide a feedback signal to control the driver. This circuit has a potential problem due to the wire delay, such that the output of the driver reaches a certain voltage level first and disables the driver, while the input of the receiver is not at the right level to switch the receiver. The possible Vt mismatch between two VSTs and the supply noise also cause a similar problem. Moreover, the floating interconnect (when the driver is disabled) is vulnerable to noise.

4.4 Low Swing Bus

Charge Inter-Shared Bus (CISB) [3] and Charge Recycling Bus (CRB) [4] are two schemes to reduce the interconnect swing by charge sharing among multiple data bit lines of a bus. Both of them can suppress the interconnect swing by a factor of n (where n is the number of bits), while the Charging Recyling Bus can produce quadratic power

savings with a factor of n^2. However, the potential power savings are offset by the full switching activity of the bus, since the bus is (dis)charged for every cycle. Both of their receivers use complicated current latch sense amplifiers, and the required timing signals adds more complexity. One stringent requirement for these bus schemes to work reliably is that all the wire capacitances shall be matched very well, which is certainly non-trivial in real system designs. The *CRB* scheme uses differential signalling while the *CISB* is single-ended. In both schemes, especially in *CRB*, the floating interconnect doesn't have good noise immunity.

4.5 Comparison

The main properties of the mentioned circuits, combined with simulated results are tabulated in Table 1. The *CMOS* scheme in the first row represents the full swing case. In general, the schemes with static drivers have better noise immunity. *PCD* is only feasible for systems with well-characterized interconnects. *CLC* scheme is very robust and can reduce energy by 60% of the original with an extra lower voltage supply. The *SDLC* scheme can reduce the energy by 70%, with low-Vt devices and two reference voltages. The *CISB* and *CRB* schemes are only suitable for multiple-bit bus units with large capacitive load. Simulation results predict energy savings of up to 3.5 times. Both of them are slow compared to other schemes due to the charge sharing mechanism. The *RSD_VST* scheme can dynamically change the swing depending on the capacitive load and the sensitivity of VST, while is susceptible to device mismatch and other noises. The *DIFF* scheme uses a very low voltage supply to achieve quadratic energy saving. However, it is not suitable (in general) for on-chip interconnection because of its double line structure and the overhead of the sense amplifier.

Schemes	Energy (PJ)	Delay (ns)	E•D (PJ•ns)	Swing (V)	Robustness	Complexity
CMOS	11.6	2.1	24.5	2.0	excellent	least
CLC	4.4	3.1	13.6	1.1	very robust	1 REF
SDLC	3.6	2.4	8.6	0.5	reliable	low-Vt devices, 2 REFs
DIFF	2.5	3.0	7.5	0.2	reliable	extra timings, 1 REF, wires doubled
PCD	3.5	2.0	7.0	0.5	only for known C_L	extra controls
RSD_VST	3.7	2.0	7.4	0.6	not reliable	1 REF, big driver
CISB	3.5	4.4	15.4	0.25	small margin, only for multi-bit bus	extra timings, sense amplifiers
CRB	3.1	3.5	10.9	0.25	not reliable, only for multi-bit bus	extra timings, wires doubled

Table 1: Performance Comparison (Vdd=2V, C_L=1PF)

5. PROPOSED INTERFACE CIRCUITS

We now present several novel or modified low-swing interconnect interface circuits to address some problems of the existing schemes. To have robust circuits, we only selected static drivers to avoid the floating interconnect. The first two schemes use regular supply voltage for the drivers, while the rest use extra low voltage supplies, which can be realized on-chip with power-efficiencies around 90% [7]. The last two schemes need additional timing signals.

5.1 Symmetric Source-follower Driver with Level Converter (SSDLC)

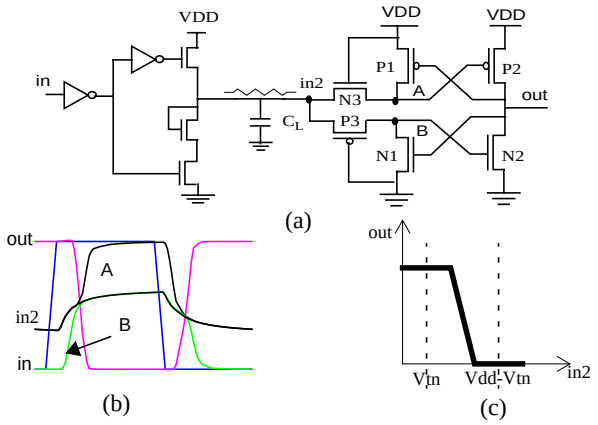

FIGURE 5. (a) Symmetric source-follower driver with level converter; (b) Simulated waveforms; (c) Voltage transform curve

The circuit of *SSDLC* scheme is shown in Fig. 5(a). The driver limits the interconnect swing from Vtn to Vdd-Vtn, shown as node *in2* in Fig. 5(b). The basic idea of the symmetric level converter is similar to the one in *SDLC* circuit, except that the gates of those two pass transistors N3 and P3 are biased at Vdd and Ground respectively. Moreover, no special low-Vt devices are needed in this circuit. Assume that node *in2* goes from low to high; Vtn to Vdd-Vtn. Initially, node A sits at Vtn and node B sits at Ground. During the transition period, with both N3 and P3 conducting, *A* and *B* rise to Vdd-Vtn as shown in Fig. 5(b). Consequently, N2 is turned on, and *out* goes to low. The feedback transistor P1 pulls *A* further up to Vdd to cut off P2 completely. *in2* and *B* stay at Vdd-Vtn. Note that there is no current path from Vdd to Ground through N3 although the gate-source voltage of N3 is nearly Vtn. Since the circuit is symmetric, the same explanation can be applied to the case of high to low transition. If ignoring feedback transistors P1 and N1, the DC voltage transform curve (VTC) of the level convertor is virtually a truncated version of that of the P2-N2 pair, as shown in Fig. 5(c). The predicted ratio of energy savings of the interconnect is defined in (EQ3):

$$\frac{E_{new}}{E_{full}} = \frac{Vdd - Vtn - Vtn}{Vdd} \qquad (EQ\ 3)$$

To obtain reasonable noise margins, Vdd is set at 2.4V in our simulation, which gives an interconnect swing of 0.7V. The sensing delay of the receiver is as small as two inverter delays. This circuit is very robust with respect to the supply noise and device variation. Moreover, no extra internal supplies are needed for this scheme.

5.2 Static Driver with VST (SDVST)

Fig. 6 shows the circuit diagram of *SDVST* scheme. The driver drives the interconnect with a swing from REF_L to Vdd-Vtn, where the threshold voltage is subject to the body effect. The internal voltage supply REF_L is set below Vtn of

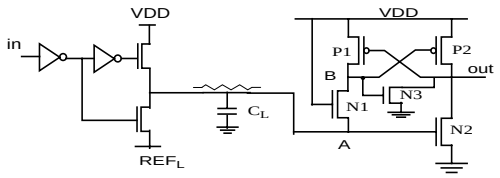

FIGURE 6. Static driver with VST

N2. The receiver is a modified version of VST, which is actually an asymmetric version of the level convertor in *SSDLC* scheme, and their operations are same in the case of low to high transition. For the case of high to low transition, after *A* and *B* are discharged to a voltage level lower than Vt of transistor N2, N2 is turned off, and P2 pulls *out* up to Vdd. Transistors P2 and N2 are sized wide enough to have large transconductances to quickly sense the small Vgs applied on them. The extra feedback transistor N3 is to provide more current drive to discharge the output. The ratio of the energy savings of the interconnect is defined as follows:

$$\frac{E_{new}}{E_{full}} = \frac{Vdd - Vtn - REF_L}{Vdd} \qquad (EQ\ 4)$$

Compared to *RSD_VST* scheme, *SDVST* is more robust because its driver is static.

5.3 Level Converter with Low-Vt Device (LCLVD)

Fig. 7 shows the schematic diagram of *LCLVD* scheme. In

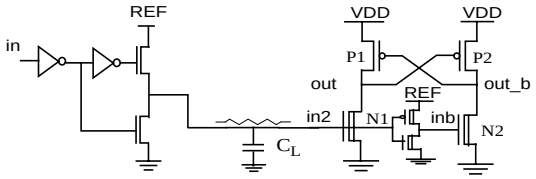

FIGURE 7. Level converter with low-Vt devices

this scheme, the receiver is the same as the one in *CCL* scheme discussed in section 4.1, except that it uses low-Vt devices for N1, N2 and the internal inverter. Because *inb* is slower than *in2*, the two branches are designed asymmetric to balance the switching delays of different directions, such as N2 is sized larger than N1, and P1 larger than P2. The ratio of energy savings is given by (EQ 5):

$$\frac{E_{new}}{E_{full}} = \left(\frac{REF}{Vdd}\right)^2 \qquad (EQ\ 5)$$

In our simulation, REF is set at 0.7V. and Vtn and |Vtp| of those low-Vt devices are set at 0.3V. This circuit is proved to be very reliable against supply noise and process variation, by the simulated results at different corners. The receiver behaves like a differential sense amplifier by regenerating a complementary input signal internally.

5.4 Capacitive-Coupled Level Converter (CCLC)

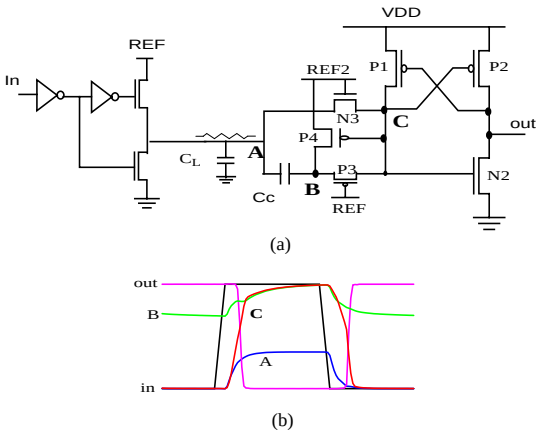

FIGURE 8. a) Capacitive-coupled level convertor; (b) Simulated waveforms

In Capacitive-Coupled Level Converter (CCLC) scheme showed in Fig. 8(a), a coupling capacitor is used to boost the low swing signal to be able to turn on the NMOS transistor of the receiver. REF2 is set to be less than (REF+Vtn). When *A* switches from high to low, pass transistor N3 is turned on, thus *C* is pulled down to Ground. *out* is pulled up to Vdd with transistor N2 turned off and P2 turned on. With pass transistor P4 conducting, *B* is set to REF2. Since the gate-source voltage cross P3 is less than its threshold voltage, P3 is not conducting, and therefore no static current path exists. When *A* goes from low to high, the coupling capacitor Cc couples a voltage jump onto *B*. Meanwhile, pass transistor N3 is turned off. *C* rises up by charge sharing with *B* through P3, as shown in Fig. 8(b). With *out* being pulled low by N2, P1 pulls *C* and *B* further up to Vdd.

The ratio of energy savings is given by (EQ 5). In our simulation, REF and REF2 are set as 0.7V and 1.2V respectively. The coupling capacitor Cc is set as 0.2PF to provide enough coupling effect for the charge sharing between Cc and parasitic capacitances, which introduces some area overhead. However, the operation of this circuit is not very sensitive to the variation of Cc. The receiver has a relatively small noise margin due to its susceptibility to the device variation.

5.5 Pseudo-DIFFerential Interconnect (PDIFF)

Fig. 9 illustrates a circuit diagram of *PDIFF* scheme. The gates of P1 and P3 are connected to *d*, while the gates of P4 and P2 are biased at Ground and REF respectively. Initially, *clk* discharges *n1*, *n2*, *A*, and *B* to Ground. After *d* is driven to the desired level, the receiver is enabled by a negative pulse of *clk*. If *d* is low, the current drive of P3 is same as that of P4, while the current drive of P1 is larger than that of P2. As a result, *B* is pulled high and *A* is pulled low. An opposite transition is triggered when *d* is high. The obvious advantage over *DIFF* scheme is that the number of wires is cut to half. However, the swing of the interconnect has to be increased to compensate the loss of immunity to common

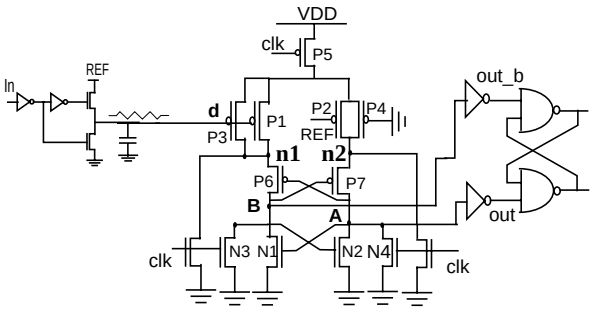

FIGURE 9. Pseudo-differential interconnect;

mode noise. The ratio of the energy savings of the interconnect is given in equation (5). REF is set at 0.6V in our simulation. The receiver is very robust against the supply noise and device variation, because of its symmetric nature with double input transistor pairs.

5.6 Level-Converting Register (LCR)

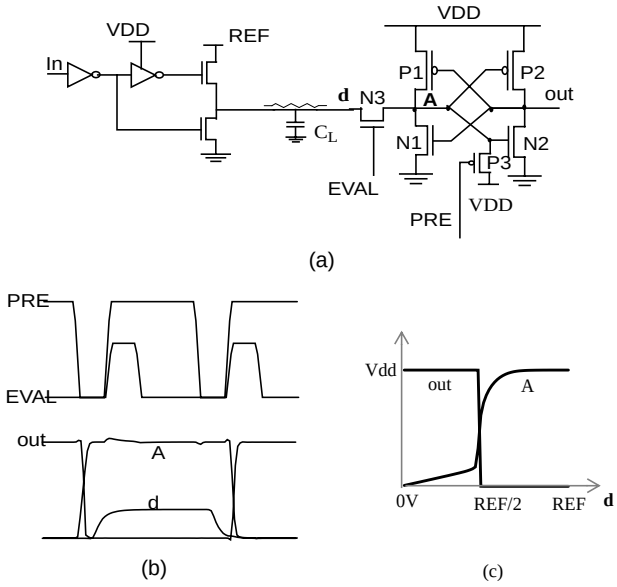

FIGURE 10. (a) Level-Converting Register; (b) simulated waveforms; (c) voltage transform curve

Fig. 10(a) shows the circuit diagram of *LCR* scheme. The receiver is just a cross-coupled inverter pair, with one precharge transistor P3 and one pass transistor N3, which gates are controlled by two timing signals PRE and EVAL respectively. The simulated waveforms are illustrated in Fig. 10(b). Initially, a negative pulse PRE is applied to P3 to precharge node *A* to Vdd and discharge node *out* to Ground. After the input signal reaches stable at node *d*, a positive pulse EVAL is applied to N3. The high end of the voltage swing of EVAL is set to be less than REF+Vtn(N3). If *d* is high, N3 stays off, and the state of the inverter pair remains the same. In the case of *d* being low, N3 starts conducting, and pulls *A* low, thus the state of the inverter pair is flipped over. After EVAL switches back to low, N3 is cut off, and the inverter pair keeps the data as a static register. The receiver is level sensitive, that when EVAL is active, the inverter pair will switch its state by a high to low glitch on the interconnect, and can not switch back by bringing the input back to high. Therefore, the EVAL pulse has to be as narrow as possible to avoid such error. Fig. 10(c) illustrates the DC voltage transform curves of the receiver, with the gate voltages of the feedback transistors P1 and N1 set to Ground. A big advantage of this simple receiver is that it combines both functions of a level converter and a register. This circuit has little area overhead, while the extra timing increases its complexity. The matching of the current drive capability of P1-N3 pair is critical for receiver's noise margin, which is susceptible to supply noise and Vt variation. However, as long as EVAL is applied after the input of the receiver reaches stable, the receiver works well. This circuit can be used for both synchronous and asychronous signalling, given the timing signals PRE and EVAL are generated correctly.

5.7 Simulation Results and Comparison

To fully compare the six proposed schemes, we have performed two sets of simulations. For all the simulations, we used the testing architecture shown in Fig. 1(a). In the first set of simulations, Vdd is set at 2V for all the schemes except for *SSDLC* scheme (Vdd=2.4V), and the capacitive load on the interconnect is swept from 0 to 5PF, with transistor sizes being kept constant. The simulation results are illustrated in Fig. 11. From the Delay vs. C_L plots, it can be seen that the proposed schemes have similar speed and their delays increase linearly with C_L with similar slopes. From the energy vs. C_L plots, we can see that their energy values increase linearly with different slopes. *LCR* scheme consumes the least. by reducing the energy with a factor of 7. *SSDLC* and *SDVST* can cut the energy by half, while *LCLVD*, *CCLC*, and *PDIFF* by a factor up to 5.The energy-delay products have a similar ranking. In the second set of simulations, C_L is set to 1PF, while the supply voltage is swept from 1.5V to 3.3V. For schemes of full swing *CMOS*, *SSDLC* and *SDVST*, the transistor sizes are kept unchanged. For others, the transistors have to be resized to optimize their operation for different supply voltages. The simulated results are illustrated in Fig. 12. *CCLC* only works well for

Schemes	Energy (PJ)	Delay (ns)	E•D (PJ•ns)	Swing (V)	Robustness	Complexity
CMOS	11.6	2.11	24.5	2.0	excellent	least
SSDLC (Vdd=2.4V)	6.89	2.73	18.8	0.7	works for variable VDDs	some area over-head
SDVST	4.79	2.38	11.4	0.7	works for variable VDDs	1 REF
LCLVD	2.43	2.49	6.05	0.7	good noise margin	Low-Vt devices, 1 REF
CCLC	2.36	2.47	5.84	0.7	small noise margin	coupling capaci-tor, 2 REFs
PDIFF	2.69	2.86	7.7	0.6	reasonable noise margin	big receiver, tim-ings, 1 REF
LCR	1.78	2.43	4.32	0.6	reasonable noise margin	timings, 2 REFs

Table 2: Performance Comparison (Vdd=2V, CL=1PF)

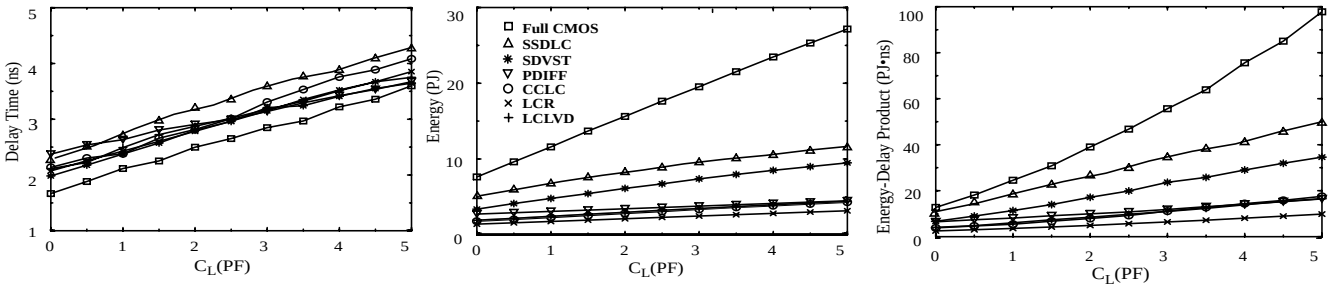

FIGURE 11. Delay, Energy, Energy-Delay product vs. Capacitive load of interconnect, at Vdd=2V

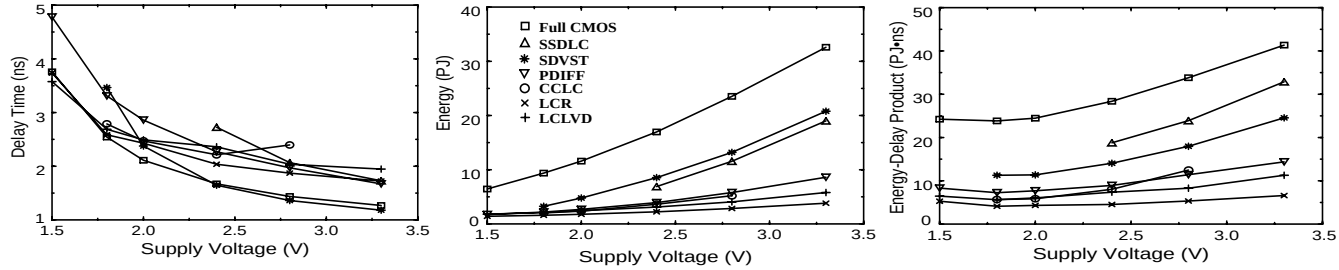

FIGURE 12. Delay, Energy, Energy-Delay product vs. Supply voltage, at C_L=1PF

Vdds between 1.8V and 2.5V, and *SSDLC* only works for Vdd higher than 2.4V. The ranking of their energy and energy-delay product are the same as in the first set of simulations. Note that *LCF*, *PDIFF*, and *LCLVD* schemes have almost flat energy and energy-delay product curves for the whole range. The performances of these schemes are tabulated in Table 2, with settings of Vdd=2V, C_L=1PF (except for *SSDLC* with Vdd=2.4V).

6. CONCLUSION

The existing low-swing interconnect interface-circuit schemes show a wide variety of problems in both efficiency, performance, and robustness. We have introduced a number of novel or modified circuits to address some of these problems, or to get even higher energy savings. The *SSDLC* and *SDVST* schemes can reduce the energy consumption up to 60% without much overhead while possessing good robustness. The *LCLVD* scheme can produce energy savings by a factor of 5 if low-Vt devices are available while also having a good noise margin. *CCLC* also gets a 5 times energy reduction without requiring extra timing signals, but comes with a large area overhead and a small noise margin. Finally, the *PDIFF* and *LCR* schemes are showing great promise for both synchronous and asynchronous system design, potentially reducing the energy by a factor of seven! In summary, low-swing interconnect is an effective tool for minimizing energy dissipation, but requires a judicious optimization with respect to robustness, design complexity, and energy reduction.

7. ACKNOWLEDGEMENTS

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