Power Dissipated by CMOS Gates Driving Lossless Transmission Lines

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***Abstract* - The dynamic and short-circuit power consumption of a CMOS gate driving an *LC* transmission line as a limiting case of an *RLC* transmission line is investigated in this paper. Closed form solutions for the output voltage and short-circuit power of a CMOS gate driving an *LC* transmission line are presented. These solutions agree with AS/X simulations within 11% error for a wide range of transistor widths and line impedances. The ratio of the short-circuit to dynamic power is less than 7% for CMOS gates driving *LC* transmission lines where the line is matched or underdriven. Therefore, the total power consumption is expected to decrease as inductance effects becomes more significant as compared to an *RC* model of the interconnect.**

I. Introduction

Interconnect has historically been modeled as a single lumped capacitance or as an *RC* impedance in the performance analysis of on-chip interconnects, see *e.g.*, [1]-[8]. Inductance, however, is becoming more important with faster on-chip transition times and longer wires [9]-[12]. Wide wires are frequently encountered in clock distribution networks and in data busses. These wires, often at the upper metal layers, are low resistance wires that can exhibit significant inductive effects [10], [11]. Furthermore, performance requirements are pushing the introduction of new materials for low resistivity interconnect [13]. In the limiting case, high temperature superconductors may possibly become commercially available [14]. More accurate *RLC* transmission line models are therefore becoming necessary in the analysis of VLSI-based interconnect. Power has also become a major design issue for portable devices and high performance microprocessors. It is therefore important to be able to estimate the effects of increasing inductance on the power consumed by a CMOS circuit.

The *RC* model can be viewed as a limiting case of the *RLC* transmission line model where the inductance is considered to be negligible. This case has been thoroughly investigated and is well represented in the literature, *e.g.*, [3]-[8]. The other limiting case is an *LC* transmission line where the resistance is negligible. This case approximates the low loss lines that are encountered in Multi-Chip Modules (MCM) and Printed Circuit Boards (PCB). Although it is highly improbable that the resistance of an on-chip interconnect will become negligible in the near term, an analysis of a lossless impedance sets an upper limit for inductance effects in VLSI circuits. The behavior of an *RLC* transmission line case can therefore be bounded by analyzing the behavior of the *RC* and the *LC* cases

The focus of this paper is the investigation of the dynamic and short-circuit power of a CMOS gate driving an *LC* transmission lines. This topic is discussed in section II. Some conclusions are offered in section III.

II. Dynamic and Short-Circuit Power

In subsection *A*, equations describing the dynamic and short-circuit power are introduced. The accuracy of these expressions are quantified in subsection *B*. In subsection *C*, the ratio of the short-circuit power to the dynamic power is discussed.

A. Power Expressions for CMOS Gates with *LC* Loads

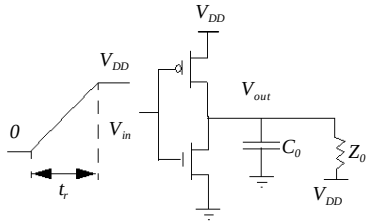

Fig. 1. An equivalent circuit of a CMOS circuit driving a lossless transmission line for $0 < t < 2T_0$.

The dynamic power consumed by a CMOS gate driving a transmission line is $P_{dyn}=C_tV_{DD}^2f$, where f is the frequency of the output, V_{DD} is the power supply, and C_t is the total capacitance of the transmission line [15]. For short-circuit power [1], the case considered here is for fast signal waveforms where the rise time is less than twice the propagation delay across the line ($t_r < 2T_0$) where T_0 is the time of flight of the signals across the line. In this case, the reflections do not affect the short-circuit power because the signal returns to the driver after the input signal has reached its final value. Under this condition, the transmission line appears as a resistance with a value Z_0. The equivalent circuit of a CMOS inverter driving a lossless transmission line for the period of time 0 to $2T_0$ is shown in Fig. 1. The short-circuit current is the current through the PMOS transistor during a rising input. The signal at the input of the CMOS driver is

$$V_{in} = kt = \frac{V_{DD}}{t_r}t\text{,} \qquad (1)$$

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before the input reaches V_{DD} (*i.e.*, $t < V_{DD}/k$).

Based on the alpha power law [16], when the PMOS transistor is in saturation the short-circuit current is [15]

$$I_{SC}(sat) = P_{Cp} \cdot \frac{W_p}{L_p} \cdot (V_{DD} - kt - |V_{Tp}|)^{\alpha_p}, \quad (2)$$

where P_C is a constant that determines the drive current of the transistor in saturation, W and L are the width and length of the transistor channel, and α is a constant between one (strong velocity saturation) and two (no velocity saturation) [16]. The suffix p indicates the PMOS transistor and the suffix n indicates the NMOS transistor. When the PMOS transistor is in the linear region, I_{SC} depends on V_{out}. Using the alpha power law model, the output voltage is [15]

$$V_{out} = V_{DD} - \frac{Z_0 \cdot P_{Cn} \cdot \frac{W_n}{L_n} \cdot (kt - V_{Tn})^{\alpha n}}{1 + \frac{P_{Cp}}{P_{Vp}} \cdot \frac{W_p}{L_p} \cdot (V_{DD} - kt - |V_{Tp}|)^{\frac{\alpha p}{2}} \cdot Z_o}, \quad (3)$$

for the time $0 < t < t_r$ and $t_r < 2T_0$. Noting that V_{DD}-V_{out} is V_{SD} of the PMOS transistor, the short circuit current of a CMOS inverter loaded by an LC transmission line is

$$I_{SC}(linear) = \frac{Z_0 \cdot P_{Cn} \cdot \frac{W_n}{L_n} \cdot (kt - V_{Tn})^{\alpha n}}{\frac{P_{Vp}}{P_{Cp}} \cdot \frac{L_p}{W_p} \cdot (V_{DD} - kt - |V_{Tp}|)^{-\frac{\alpha p}{2}} + Z_o}. \quad (4)$$

B. Accuracy of Power Expressions

A CMOS gate driving a transmission line can be characterized by the impedance matching factor λ, where

$$\lambda = \frac{2S_p W_p Z_0}{V_{DD}}. \quad (5)$$

When $\lambda = 1$, the transistor is optimally matched to the transmission line. If λ is less than one, the transmission line is underdriven and the response suffers from a slow output rise time. If λ is greater than one, the transmission line is overdriven and the response suffers from overshoots and undershoots that can cause reliability problems. Thus, the range defined by $0.3 < \lambda < 1.6$ is arbitrarily chosen to be the range of interest. The analytical solutions of (2) and (4) are compared to AS/X simulations [18] in Fig. 2 assuming $t_r = 100$ *ps* and using λ as a parameter. The analytical solution shows good agreement with the simulations for a wide range of λ.

The short-circuit energy per transition can be calculated from

$$E_{SC} / Transition = Area_{SC} \cdot V_{DD}, \quad (6)$$

where $Area_{SC}$ (in coulombs) is the area under the short-circuit current curve. This area can be approximated by a triangle [7] whose base is given by $(V_{DD}-V_{Tn}+V_{Tp})t_r/V_{DD}$ and height is given by I_{peak} (the maximum point on the short-circuit current curve). Thus, the short-circuit energy per transition is

$$E_{SC} / Transition = \frac{I_{peak}}{2}(V_{DD} - V_{Tn} - |V_{Tp}|)t_r K_c, \quad (7)$$

where K_c is a constant correction factor [15].

I_{peak} can be calculated by equating (2) and (4). Alternatively, I_{peak} can be calculated as

$$I_{peak} = K(\lambda) W_p, \quad (8)$$

where $K(\lambda)$ is determined from varying λ and calculating I_{peak}/W_p, as plotted in Fig. 3.

$K(\lambda)$ represents in I_{peak} the effect of the output waveform on the short-circuit current [15]. AS/X simulations are compared to (7) in Table 1. The analytical solution shows good agreement (less than 1% error for $\lambda > 1$) with the circuit simulations for a wide range of λ and exhibits a maximum error of 11% for small λ.

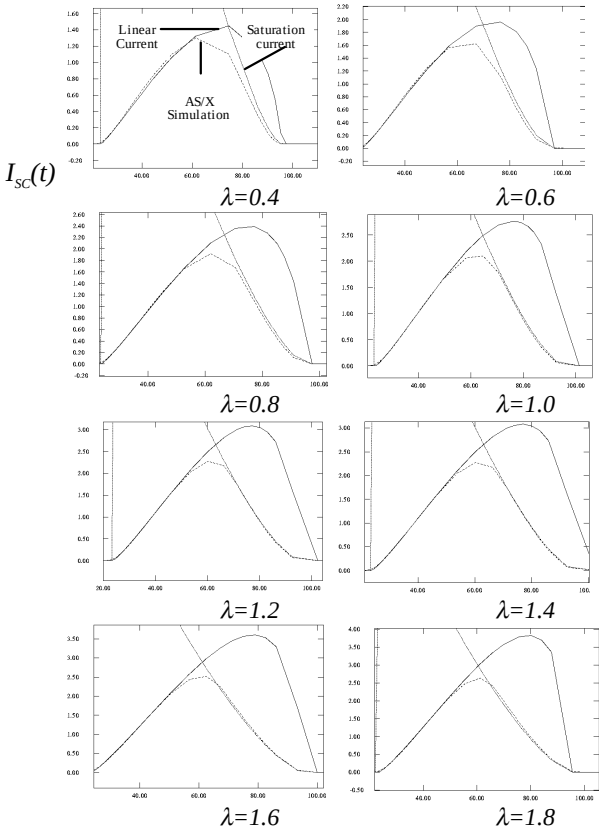

Fig. 2. Analytical solutions for short-circuit current in (2) and (4) compared to AS/X simulations for different values of λ.

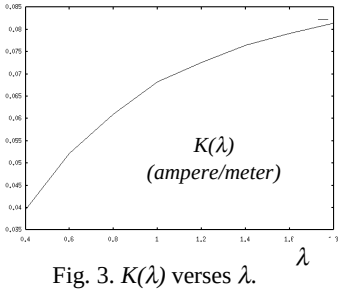

Fig. 3. $K(\lambda)$ verses λ.

Table 1: Short-circuit energy per transition as a function of λ. AS/X simulations are compared to analytical solutions. (E_{SC}/transition in joules)

λ	AS/X Simulation x10^{-15}	Analytical x10^{-15}	% Error
0.4	131.20	116.00	11.00
0.6	161.45	152.50	5.50
0.8	182.77	178.95	2.09
1.0	199.60	199.60	0.00
1.2	212.55	212.30	0.12
1.4	224.55	223.20	0.60
1.6	231.93	231.37	0.24
1.8	239.68	238.20	0.62

C. Short-Circuit to Dynamic Power Ratio

Assuming a symmetric CMOS gate, the short-circuit power is

$$P_{SC} = I_{peak}(V_{DD} - V_{Tn} - |V_{Tp}|)t_r f \cdot \quad (9)$$

As described previously, the dynamic power is

$$P_{dyn} = \frac{T_0}{Z_0} \cdot {V_{DD}}^2 f \text{ ,} \quad (10)$$

where T_0/Z_0 is equal to C_t [15]. Dividing (9) by (10), the magnitude of the dynamic power can be compared to the magnitude of the short-circuit power. The resulting ratio is

$$\frac{P_{SC}}{P_{dyn}} = K(\lambda)\lambda \cdot \frac{(V_{DD} - V_{Tn} - |V_{Tp}|)}{V_{DD}} \frac{t_r}{T_0} \cdot \frac{K_c}{2S_p} \cdot \quad (11)$$

The ratio between the short circuit power and the dynamic power depends upon the matching condition of the transmission line to the CMOS gate (λ) and the ratio between the rise time of the input signal to the time of flight of the waves across the transmission line (t_r/T_0). The dependence on the supply voltage is fairly weak. The dependence exists only if the supply voltage and the threshold voltages scale differently. The dependence of the short-circuit to dynamic power ratio on λ is shown in Fig. 4. As the matching condition moves from underdriven to matched to overdriven, the short-circuit to dynamic power ratio increases. This ratio is less than 7% for the matched ($\lambda = 1$) and underdriven cases ($\lambda < 1$) [15]. The classical design criteria for driving a capacitive load is to maintain equal input and output transition times which gives rise to a short-circuit power of approximately *20%* of the dynamic power [1]. For *RC* loads, the P_{SC}/P_{Dyn} ratio is even higher. Thus, the total power consumption is expected to decrease as inductance effects increase.

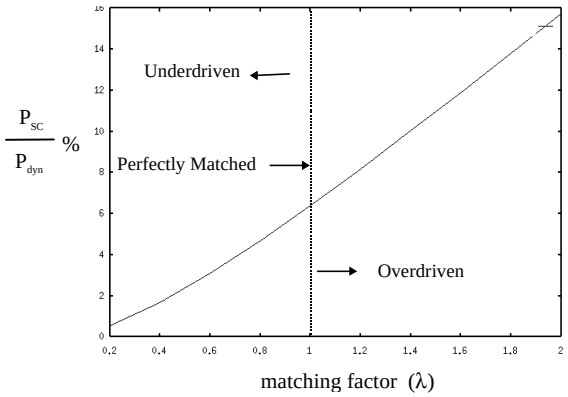

Fig. 4. Dependence of short circuit to dynamic power ratio on λ.

III. Conclusions

The dynamic power consumed by a CMOS gate driving a lossless transmission line is investigated. It is shown that the dynamic power of a CMOS gate driving a lossless transmission line is the same as that of a CMOS gate driving a capacitor equal to the total capacitance of the line. A closed form solution for the short-circuit power is presented that agrees with circuit simulations within 11% error for a wide range of the matching factor λ. An expression for the short-circuit to dynamic power ratio is presented that shows that the short-circuit power is below 7% of the dynamic power for λ less than or equal to one. Thus, the short-circuit power for the case of an *LC* load is much less than that of the case of an *RC* load. In the case of an *RLC* load, the short-circuit power is in the middle, greater than the case of an *LC* load but less than the case of an *RC* load.

References

[1] H. J. M. Veendrick, "Short-Circuit Dissipation of Static CMOS Circuitry and its Impact on the Design of Buffer Circuits," *IEEE Journal of Solid-State Circuits*, Vol. SC-19, No. 4, pp. 468 - 473, August 1984.

[2] S. R. Vemuru and N. Scheinberg "Short-Circuit Power Dissipation Estimation for CMOS Logic Gates," *IEEE Transactions on Circuits and Systems*, Vol. CAS-41, No. 11, pp. 762 - 765, November 1994.

[3] S. Bothra, B. Rogers, M. Kellam, and C. M. Osburn "Analysis of the Effects of Scaling on Interconnect Delay in ULSI Circuits," *IEEE Transactions on Electron Devices* Vol. ED-40, No. 3, pp. 591 - 597, March 1993.

[4] T. Sakurai, "Approximation of Wiring Delay in MOSFET LSI," *IEEE Journal of Solid-State Circuits*, Vol. SC-18, No. 4, pp. 418 - 426, August 1983.

[5] E. G. Friedman and J. H. Mulligan, "Ramp Input Response of *RC* Tree Networks," *Analog Integrated Circuits and Signal Processing*, Vol. 14, No. 1/2, pp. 53-58, September 1997.

[6] L. V. Ginneken, "Buffer Placement in Distributed RC-tree Networks for Minimal Elmore Delay," *Proceedings of the IEEE International Symposium on Circuits and Systems*, pp. 865 - 868, May 1990.

[7] V. Adler and E. G. Friedman, "Delay and Power Expressions for a CMOS Inverter Driving a Resistive-Capacitive Load," *Analog Integrated Circuits and Signal Processing*, Vol. 14, No. 1/2, pp. 29 - 39, September 1997.

[8] J. Rubinstein, P. Penfield, and M. Horowitz, "Signal Delay in *RC* Tree Networks," *IEEE Transactions on Computer-Aided Design*, Vol. CAD-2, No. 3, pp. 202 - 211, July 1983.

[9] D. A. Priore, "Inductance on Silicon for Sub-Micron CMOS VLSI," *Proceedings of the IEEE Symposium on VLSI Circuits*, pp. 17-18, May 1993.

[10] A. Deutsch *et al.*, "Modeling and Characterization of Long Interconnections for High-Performance Microprocessors," *IBM Journal of Research and Development*, Vol. 39, No. 5, pp. 547 - 667, September 1995.

[11] A. Deutsch *et al.*, "When are Transmission-Line Effects Important for On-Chip Interconnections?," *IEEE Transactions on Microwave Theory and Techniques*, Vol. MTT-45, No.10, pp. 1836-46, October 1997.

[12] Y. I. Ismail, E. G. Friedman, and J. L. Neves, "Figures of Merit to Characterize the Importance of On-Chip Inductance," *Proceedings of the IEEE/ACM Design Automation Conference*, June 1998.

[13] J. Torres, "Advanced Copper Interconnections for Silicon CMOS Technologies," *Applied Surface Science*, Vol. 91, No. 1, pp. 112 - 123, October 1995.

[14] K. K. Likharev and V. K. Semenov, "RSFQ Logic/Memory Family: A New Josephson-Junction Technology for Sub-Terahertz-Clock Frequency Digital System," *IEEE Transactions on Applied Superconductivity*, Vol. AS-1, No. 1, pp. 3 - 28, March 1991.

[15] Y. I. Ismail, E. G. Friedman, and J. L. Neves, "Dynamic and Short-Circuit Power of CMOS Gates Driving Lossless Transmission Lines," *Proceedings of the IEEE Great Lakes Symposium on VLSI*, pp. 39-44, February 1998.

[16] T. Sakurai and A. R. Newton "Alpha-Power Law MOSFET Model and its Applications to CMOS Inverter Delay and Other Formulas," *IEEE Journal of Solid-State Circuits*, Vol. SC-25, No. 2, pp. 584 - 593, April 1990.

[17] L. N. Dworsky, *Modern Transmission Line Theory and Applications*, John Wiley & Sons, Inc., New York, 1979.

[18] *AS/X User's Guide*, IBM Corporation, New York, 1996.