A High Speed and Low Power SOI Inverter using Active Body-Bias

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ABSTRACT

We propose a new high speed and low power SOI inverter that can operate with efficient body-bias control and free supply voltage. The performance of the proposed circuit is evaluated by both the BSIM3SOI circuit simulator and the ATLAS device simulator, and then compared with other reported SOI circuits. The proposed circuit is shown to have excellent characteristics. At the supply voltage of 1.5V, the proposed circuit operates 27% faster than the conventional SOI circuit with the same power dissipation.

Keywords

SOI inverter, low power, dynamic threshold, body-bias

1. INTRODUCTION

One of the main approaches to low power consumption is to reduce the supply voltage. Reducing the supply voltage should be accompanied by a threshold voltage reduction, and the reduction of the supply voltage is limited by the amount of the off-state leakage current. One solution to this problem is a dynamic threshold operation which applies an active body-bias to MOSFETs[1]. Because of low threshold voltage during the logic transition and high threshold voltage during the off-state, the dynamic threshold circuit operates at high speed with low power.

The body of an SOI MOSFET can be easily isolated from other electrical nodes, which makes the dynamic threshold scheme possible by applying an independent body-bias. Several SOI dynamic threshold circuits have been proposed recently (Figure 1) [1]-[4].

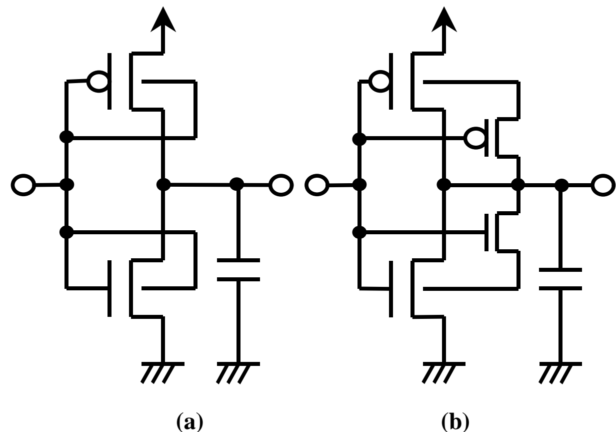

Figure 1: Reported SOI inverter circuits; (a) [1], (b) [2].

In this paper, we propose a new scheme of a high speed, low power SOI inverter using active body-bias. The proposed circuit is evaluated and compared with other schemes by both circuit simulation and device simulation. Also, the dependence of the circuit performance on the body resistance of the MOSFETs is evaluated.

2. CIRCUIT DESCRIPTION

The proposed inverter circuit is shown in Figure 2. The bodies of the main MOSFETs, Mn and Mp, are connected to the sources of the subsidiary MOSFETs, Mn^* and Mp^*, respectively. The subsidiary MOSFETs are designed to be small. The additional input capacitance increase is only the junction capacitance of the subsidiary MOSFET.

Figure 3 compares the layouts of the proposed inverter and the conventional SOI inverters with T-gate structure and source-body tie structure body contact. For compact layout of the proposed inverter, T-gate devices are used and the body of the main MOSFET and the source of the subsidiary MOSFET is connected with the contact-silicide. In the conventional SOI inverter, it can be seen that Figure 3(c) is more compact than Figure 3(b).

The widths of all subsidiary MOSFETs (Mn^* and Mp^*) in the simulation are 1μm and that of the main MOSFETs(Mn and Mp) are 12μm and 24μm, respectively. In comparison, 14μm(N) and 28μm(P) devices in the conventional SOI were used in simulation for the same total area.

The pull-down operation of the proposed inverter is as follows (Figure 4).

When IN is "L" and OUT is "H", Mn is off and Mn^* is on. At this time, the body potential of Mn is "L". When IN changes from "L" to "H", both Mn and Mn^* are on simultaneously. The body potential of Mn becomes charged up to the diode turn-on voltage of about 0.7V soon after the pull-down begins (region A in Figure 4). The lowered threshold voltage of Mn enhanced the drain current and the pull-down transition time is reduced. Also, the higher channel mobility[1] and parasitic bipolar action[2] contribute to the enhanced performance. As OUT goes down, the body potential of Mn decreases because some channel electrons of Mn^* are injected into the body of Mn and recombined with the holes and also because of the drain-to-body capacitive coupling of Mn (region B).

When IN changes from "H" to "L" during pull-up, initially the body potential of Mn decreases abruptly due to the floating body effect because Mn^* is off at this time and

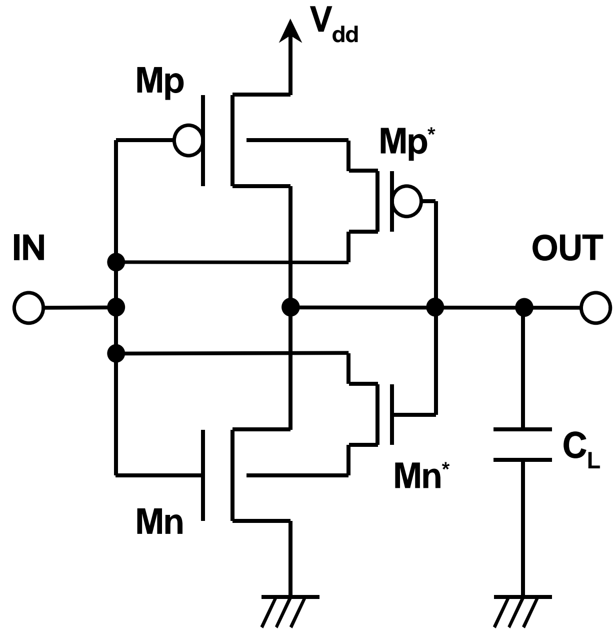

Figure 2: The proposed circuit scheme. Mn and Mp are the main MOSFETs. Mn* and Mp* are the subsidiary MOSFETs.

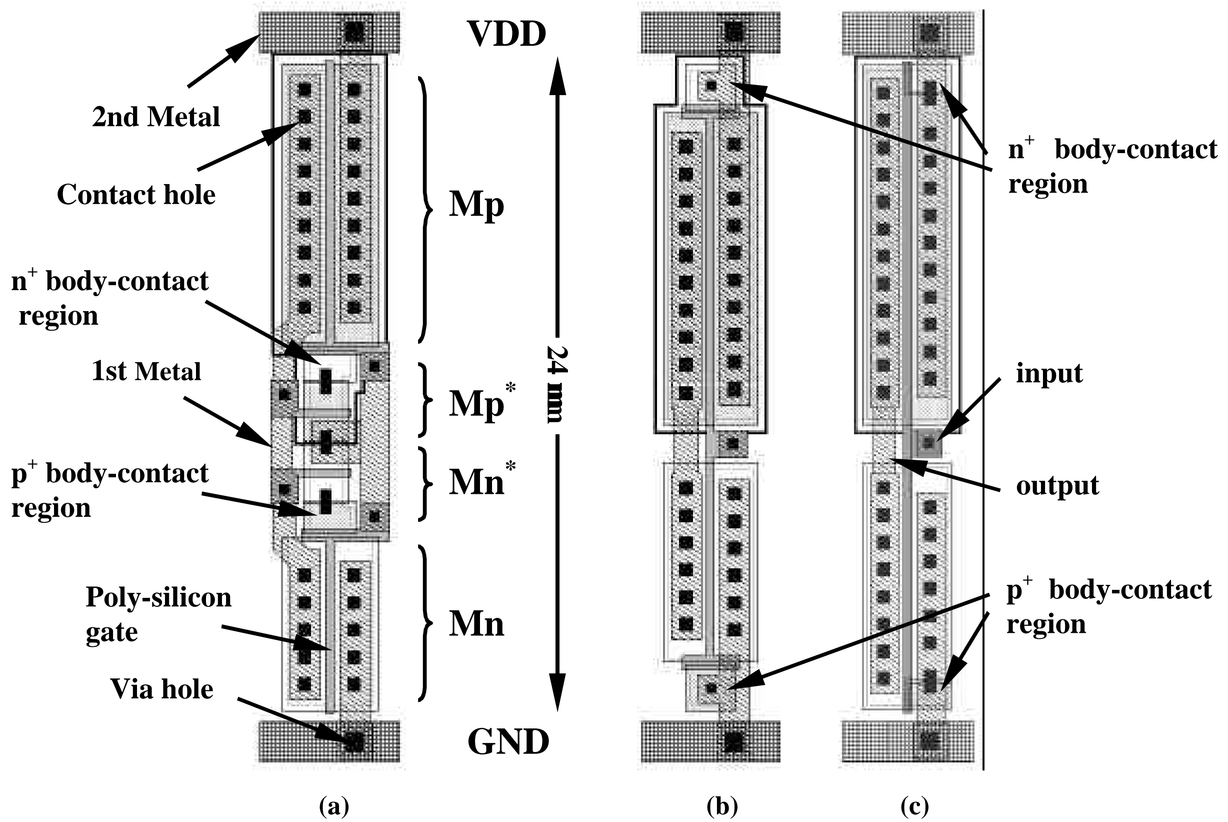

Figure 3: Comparison of the layouts. (a) The proposed inverter. (b) The conventional SOI inverter with T-gate structure body contact. (c) The conventional SOI inverter with source-body tie structure body contact.

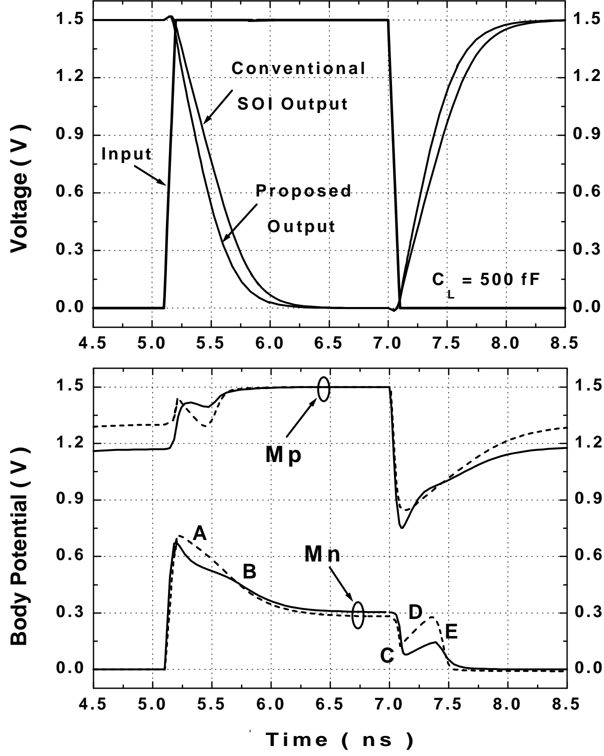

Figure 4: OUT and body nodes transient waveforms of the proposed circuit. The effective gate length of all MOSFETs is 0.25 mm and the width of PMOSFET is twice that of NMOSFET. The solid line and the dashed line are the results from circuit simulation and device simulation, respectively.

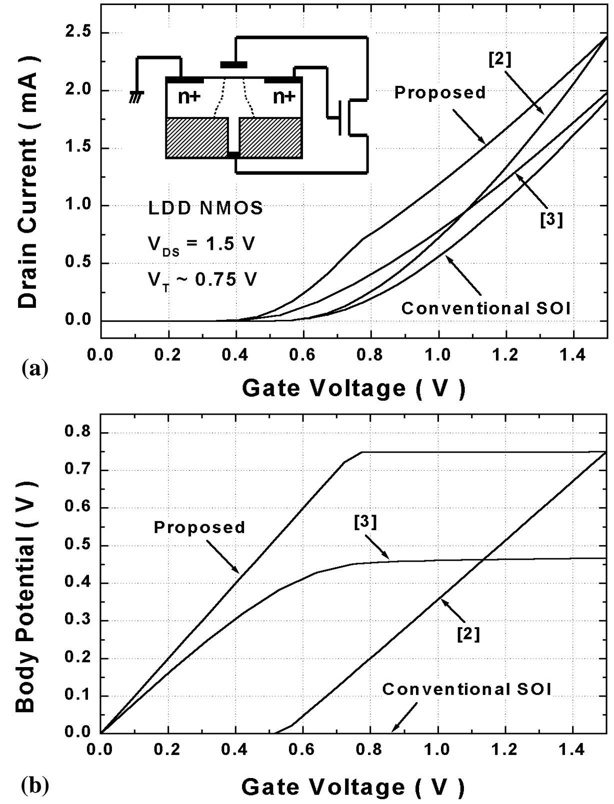

Figure 5: The I_D-V_{GS} characteristics of the pull-down stage obtained by device simulation. The silicon film thickness in the simulation domain is 200 nm. (a) Drain current. (b) Body potential.

therefore the body of Mn is floating (region C)[5]. As OUT increases, the body potential increases due to the drain-to-body capacitive coupling (region D). When OUT goes up above the V_T of Mn^*, Mn^* turns on and the body potential of Mn returns to "L" (region E).

The operation of the PMOSFETs can be explained symmetrically.

3. SIMULATION RESULTS

We used the BSIM3SOI circuit simulator[8] and ATLAS two dimensional device simulator[9] to simulate the proposed circuit, and compared the performance with other circuits.

The transient waveforms of the output and the body potential of the main MOSFETs were compared with those of the conventional SOI inverter in Figure 4. The initial body potential increase in the main MOSFETs is close to 0.7V.

Figure 5 shows the I_D-V_{GS} characteristics of the pull-down stage. The data were obtained by mixed-mode simulation. The insert is the simulation domain of the pull-down stage. From this, we were able to observe the superior I-V characteristics of the proposed scheme. The proposed circuit had the lowest input threshold voltage and the highest body potential compared with the other schemes, which led to the highest speed.

To check the AC performance and how the supply voltage affects the delay time and power dissipation, 7-stage inverter chains were simulated at C_{int}=70fF and C_L=200fF (Figure 6). At the supply voltage of 1.5V, the proposed circuit operated 27% faster than the conventional circuit with almost the same power dissipation. The proposed circuit also ran 13% faster than the circuit in [2] because our circuit had smaller input capacitance, smaller input threshold of the Mn^*, and higher body potential. Also, the circuit in [3] requires two more MOSFETs than our proposed circuit. As the supply voltage decreased, the speed advantage of our circuit increased. At the supply voltage of 1.2V, the proposed circuit had the speed merit of 35% and 20% over the conventional circuit and the circuit in [2], respectively.

Figure 7 compares the delay time per stage of the ring oscillators. The insert shows the transient waveform of our circuit at V_{dd} of 1.5V. Again, our circuit had the best speed characteristics.

Figure 8 shows how the load capacitance affected the delay time and power dissipation at 1.5V. As the load capacitance increased, the advantages of the proposed circuit over the conventional SOI also increased. The proposed circuit operated 20% faster at 100fF and 23% faster at 700fF than the conventional SOI.

4. DESIGN INSIGHT

Figure 9 shows how the body resistance on the main MOSFETs affected the delay time. As the body resistance increased, the speed performance degraded. To limit the delay time increase due to the body resistance less than 5%, the body resistance should be kept below 3 kΩ/□.

In the previous study, very large ΔV_t can be obtained by using the retrograde-doping[6]. How the doping engineering affected the circuit performance is shown in Figure 10. The current drivability of the retrograde doped inverter was dramatically enhanced compared with that of the uniformly doped inverter due to the higher body effect factor. Also note that the retrograde-doping results in reduced the body resistance.

Consequently, to reduce the body resistance and maximize ΔV_t, retrograde-doping engineering is recommended.

Figure 11(a) shows the proposed circuit diagram of NAND gate as one of applications of the proposed scheme. The gates of all subsidiary MOSFETs in series network should be connected to the output node for both the subsidiary MOSFETs to operate effectively. When V_B changes of the fixed V_A of 1.5V, resultant output waveforms for both the proposed and the conventional circuits are shown in Figure 11(b). It can be seen that speed of the proposed NAND circuit is superior to that of the conventional SOI circuit.

5. CONCULSION

We have proposed a new scheme of high speed and low power SOI inverter using an active body-bias. The operation and performance of the circuit was evaluated by BSIM3SOI and ATLAS simulation. The proposed circuit shows excellent characteristics for high speed and low power applications.

The proposed circuit also can be applied to the general CMOS logic circuits and CPL(complementary pass-transistor logic) gates for low power applications.

ACKNOWLEDGMENTS

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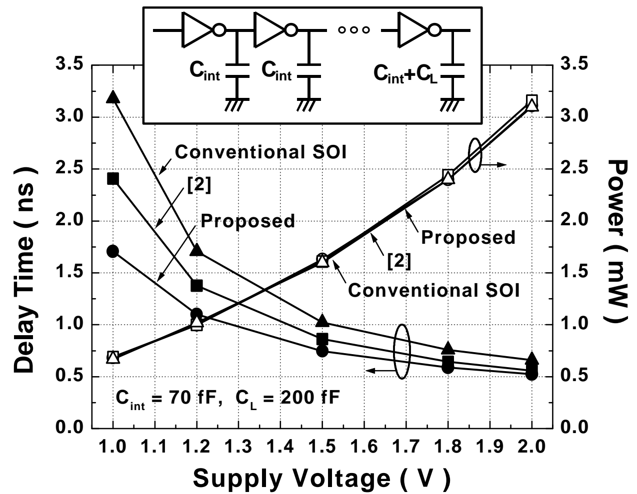

Figure 6: Delay time and power dissipation of 7-stage inverter chains at 100 MHz.

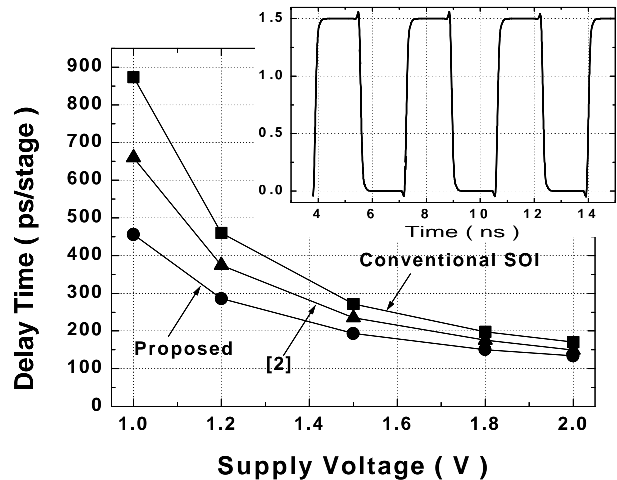

Figure 7: Delay time per stage of a ring oscillator with 17 inverters at C_{int}=70 fF.

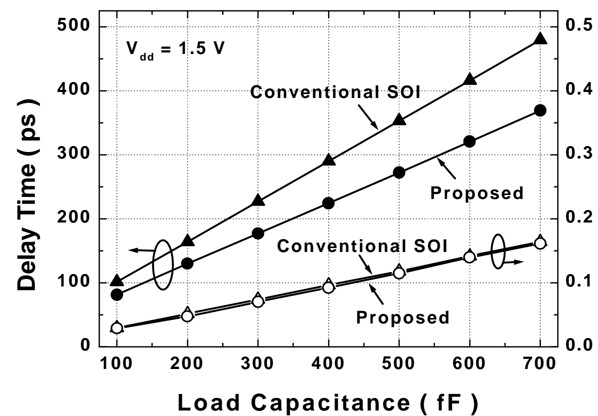

Figure 8: Load capacitance dependence of delay time and power dissipation at V_{dd} of 1.5 V.

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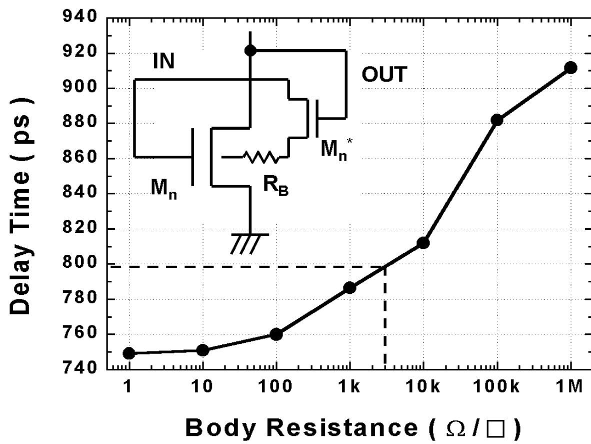


Figure 9: The body series resistance dependence of the delay time.

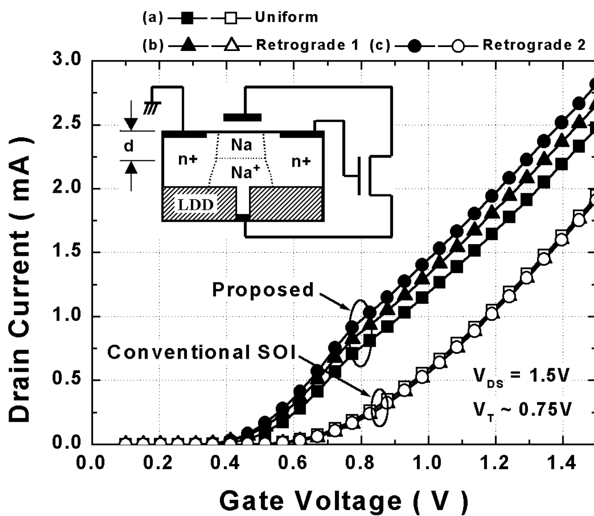
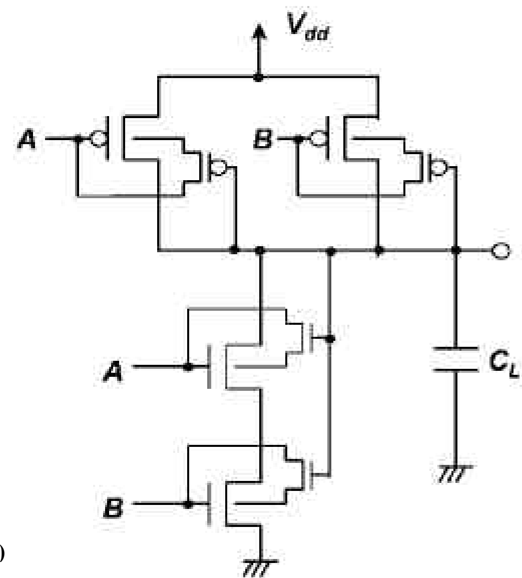


Figure 10: The current drivability of the various channel doping engineering obtained by device simulation. Device parameters are (a) $N_A=2.5\times10^{17}$ cm^{-3}; (b) $N_A=2\times10^{17}$ cm^{-3}, $N_A^+=1\times10^{18}$ cm^{-3}, d=55 nm; and (c) $N_A=2\times10^{17}$ cm^{-3}, $N_A^+=1\times10^{19}$ cm^{-3}, d=60 nm.



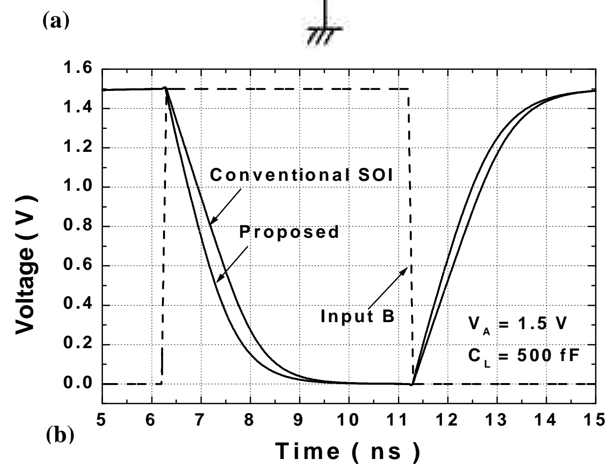


Figure 11: (a) The proposed circuit diagram of NAND gate. (b) The transient waveform. Device sizes are as follows: $(W/L)_{main}$= 7/0.25 μm and $(W/L)_{subsidiary}$= 1/0.25 μm for the proposed circuit, $(W/L)_{N,P}$ = 9/0.25 μm for the conventional SOI circuit.