A Delay Distribution Squeezing Scheme with Speed-Adaptive Threshold-Voltage CMOS (SA-Vt CMOS) for Low Voltage LSIs

Masayuki Miyazaki, Hiroyuki Mizuno, and Koichiro Ishibashi
Central Research Laboratory, Hitachi, Ltd., Kokubunji, Tokyo, 185-8601 JAPAN

mmiya@crl.hitachi.co.jp

Abstract

In a speed-adaptive threshold-voltage CMOS (SA-Vt CMOS) circuit, the substrate bias is controlled so that delay in the circuit stays constant. Distributions of device speeds are squeezed under fast-operation conditions. With a ring oscillator using 0.25-μm CMOS devices as a test circuit, we found that the worst-case operating frequency was improved from 20 MHz to 55 MHz, and the fluctuation of the operating frequency was suppressed from 44 % to 15 % while the supply-voltage variation was under 0.1 V with a 1.8 V supply voltage.

1. Introduction

CMOS LSI performance has increased as the device feature sizes have decreased. However, device deviations and operating-condition variations will limit the performance increase. This paper describes a new circuit technique that overcomes this problem. Although conventional schemes control the substrate bias so that leakage current becomes constant [1] or $V_{dd} = 3V_{th}$ [2], the proposed scheme controls the bias so that the delay in the circuit stays constant. As a result, the distributions of device speeds are squeezed under fast-operation conditions. And also, this speed-adaptive threshold-voltage CMOS (SA-Vt CMOS) becomes effective at low supply voltage operation. The digital delay locked loop used in this work realizes stable operation.

2. SA-Vt CMOS Scheme

The concept of SA-Vt CMOS is shown in Fig. 1. The circuit is composed of a delay line controlled through the threshold voltage (V_{th}), a delay-fluctuation detector, and a substrate-bias (V_{bb}) generator. The delay of the 200 series inverters in the V_{th}-controlled delay line is managed through the substrate bias. The delay-fluctuation detector measures the delay from an external clock signal to an

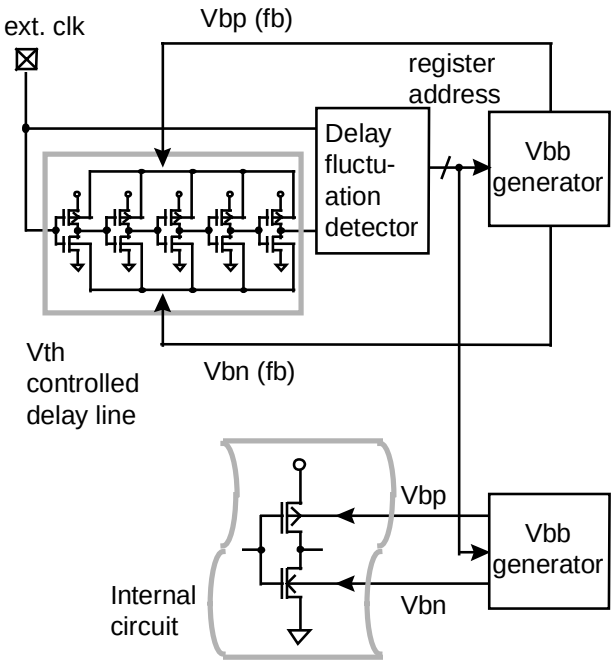
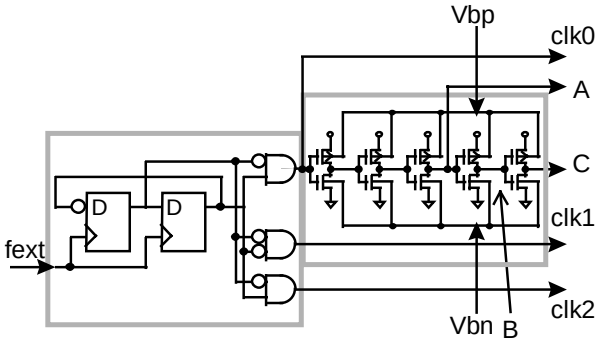
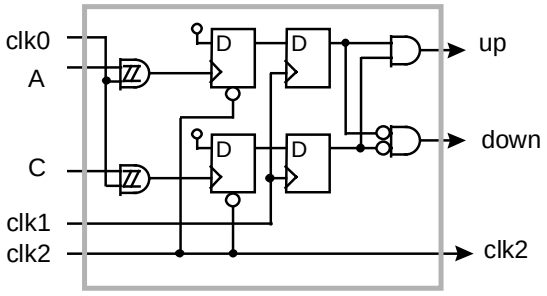


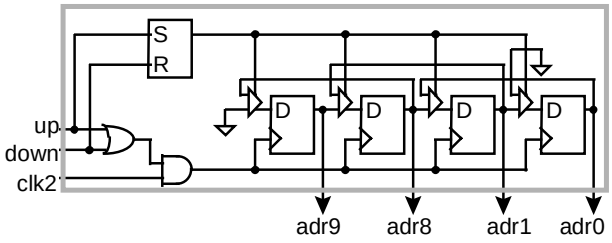
Figure 1. Concept of the SA-Vt CMOS system.



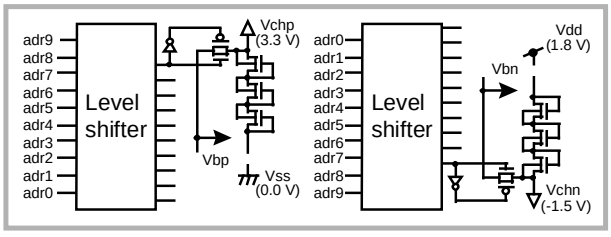
(a) Clock pulse generator and Vth controlled delay line.



(b) Delay comparator.



(c) U/D register.



(d) Vbb generator.

Figure 2. The SA-Vt CMOS circuit.

output signal of the delay line and converts the amount of delay into a register address. The V_{bb} generator supplies substrate bias voltages (V_{bp} and V_{bn}) to the delay line and internal circuits according to the register address. The delay line, the delay-fluctuation detector, and the V_{bb} generator form a feedback loop that is stable when the delay of the delay line corresponds to the external clock.

Figure 2 shows a circuit diagram of the SA-Vt CMOS in detail. A 100-MHz clock is put into the SA-Vt CMOS as clock signal, f_{ext}. A clock pulse generator divides the frequency of f_{ext} into four and produces three clock signals clk0, clk1,and clk2 which appear at different phases (with duty ratio of 1/4) as shown in Fig. 3. The rising edges of delay signals A, B, and C in the V_{th}-controlled delay line are compared

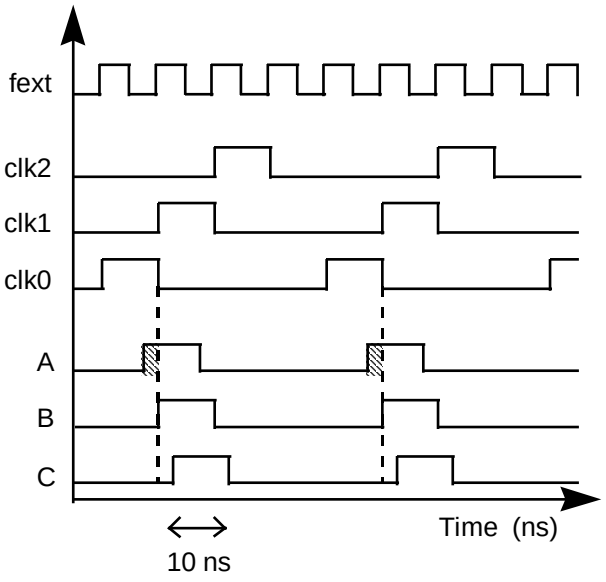
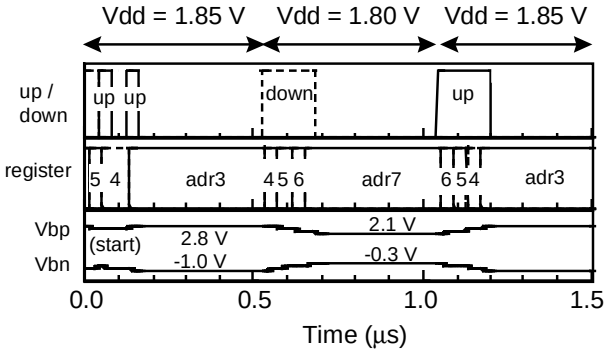
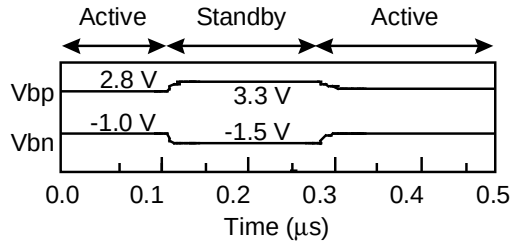


Figure 3. Timing chart of clock signals.



(a) Supply voltage fluctuation.



(b) Active / standby mode transition.

Figure 4. Simulated results of delay time compensation.

w

with the falling edge of clk0. The falling edge of clk0 must be held between the rising edges of delay signals A and C after the feedback-loop system becomes stable. In case some condition change occurs, the delay of the delay line varies, and a delay comparator sends an UP or DOWN signal. In an U/D register, only one address signal becomes an "H" level. The "H" address is increment or decrement when the UP or DOWN signal is received. The address signal controls the switches in the V_{bb} generator which provides the substrate biases. The substrate biases V_{bp} and V_{bn} produced at the V_{bb} generator are supplied to the delay line and changed so that the delay of the delay line becomes a pre-determined time. The oscillation problem of this feedback loop system is avoided because the charge time of the delay-line substrate is fast enough for the 40-ns UP/DOWN cycle of the register signal transition. That is, the system operates stably because the feedback of the substrate for the delay line (V_{bp}(fb), V_{bn}(fb)) is isolated from that for internal circuits. Figure 4 shows the simulated results of the delay compensation with the substrate bias control. The settling time is 160 ns, when the supply voltage (V_{dd}) varies between 1.80 V and 1.85 V as the output signal changes from register3 to register7. The switching time of the SA-Vt CMOS from the standby state to the active state is fast because the U/D register memorizes the delay at one of the registers. The switching time is 40 ns.

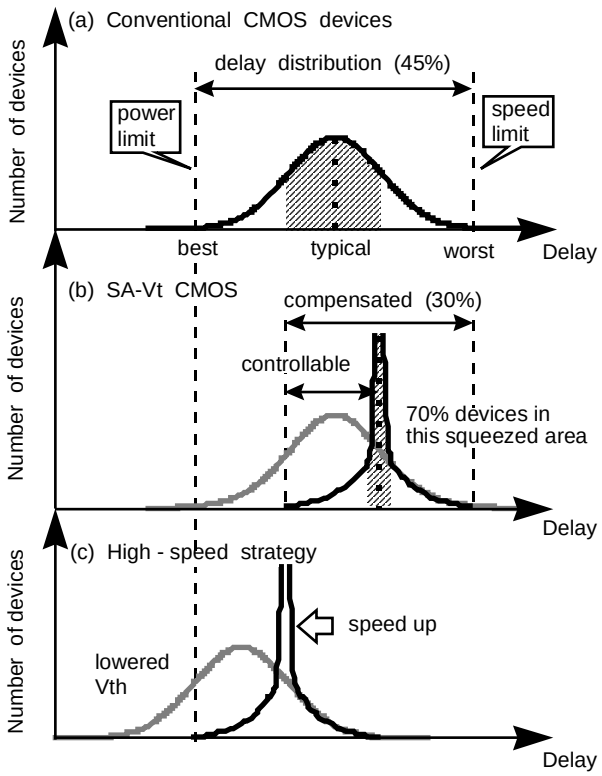


Figure 5. Strategy for high-speed operation with delay control.

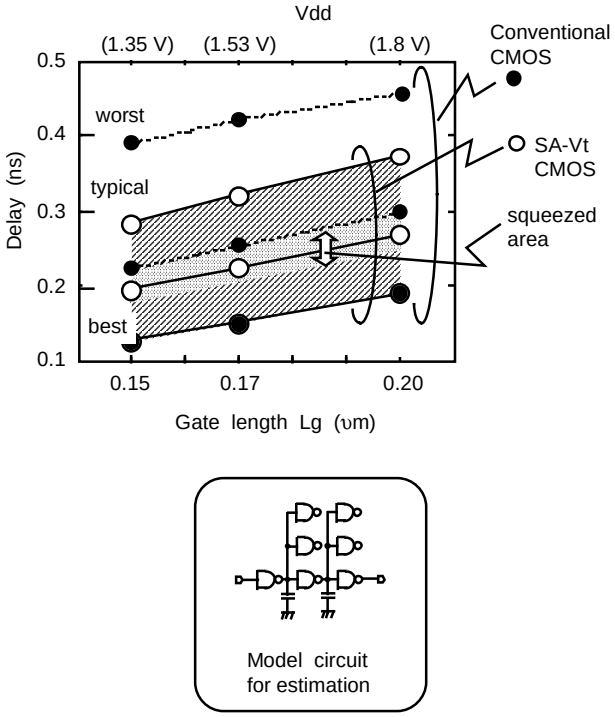


Figure 6. Delay trend with device feature size.

3. High Speed Operation

A strategy for high-speed operation is shown in Fig. 5. As shown in Fig. 5(a), the delay of conventional CMOS devices changes from the best condition to the worst. The best condition is limited by the pre-determined leakage power dissipation and the worst condition is limited by speed. The range of the delay distribution depends on the variation of V_{dd}, operating-temperature transition, and device-parameter deviations. For 0.20-μm CMOS devices, for example, the distribution width is 45% as shown in Fig. 5(a). The maximum substrate bias determines the controllable area. If a 1.8-V substrate bias is supplied, the SA-Vt control will squeeze (narrow) the distribution of 70% CMOS devices. As a result, the SA-Vt CMOS will compensate the distribution into 30% as shown in Fig. 5(b). Taking into account the effect of the SA-Vt control, devices can be fabricated with V_{th} lower than the leakage power limitation. As illustrated in Fig. 5(c), the SA-Vt CMOS increases the speed of the CMOS devices within that allowed by the power dissipation limit.

Figure 6 shows the simulated results of delay for different device feature sizes. A 3-fan-in 3-fan-out gate delay is used and a constant-field scaling rule is applied for this simulation. Dotted lines describe the conventional CMOS device delay. The effect of the SA-Vt CMOS is shown in the shaded area in this

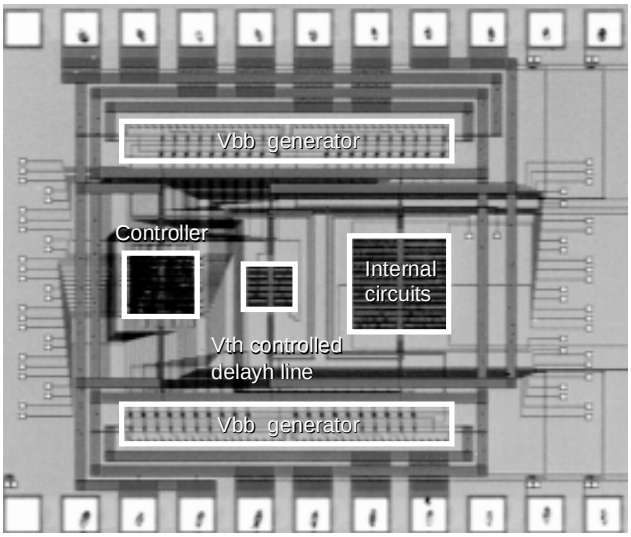


Figure 7. Chip micriggraph.

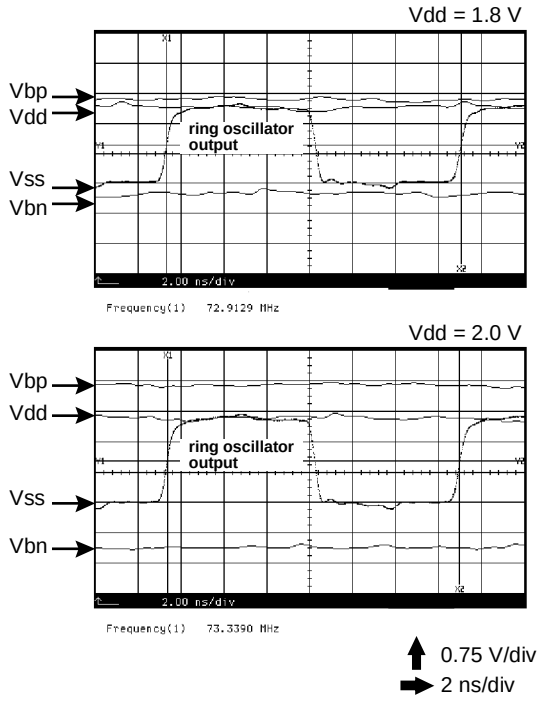


Figure 8. Measured waveforms of a ring oscillator as a test circuit controlled by SA-Vt CMOS.

figure. Especially, the speeds of 70% devices are squeezed and distributed in the dark area. The worst delay of the devices decreased by 18% at 0.20-μm, 23% at 0.17-μm, and 27% at 0.15-μm gate lengths. Thus, the effect of SA-Vt CMOS increases as the gate length is decreased toward 0.1μm level.

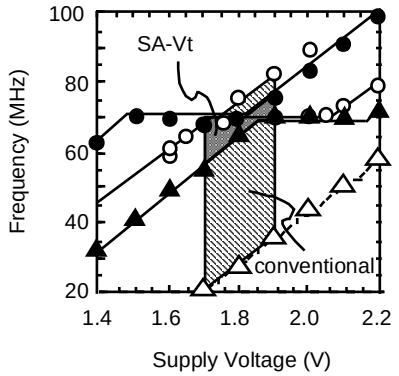
4. Experiments and Results

We fabricate the SA-Vt CMOS by using the 0.25-μm CMOS process with 5 layers of interconnection metal. The gate oxide thickness of the MOS FET was 4.5 nm. The chip micrograph of the SA-Vt CMOS is shown in Fig. 7. The V_{th}-controlled delay line occupies 100x100μm, the V_{bb} generator occupies 660x140μm, and the other components occupy 135x135μm. The total area of the SA-Vt CMOS is $1.2x10^5 \mu m^2$. We measured a 53-stage ring oscillator as an SA-Vt controlled internal circuit. The measured waveforms are shown in Fig. 8. When V_{dd} increases, V_{bp} and V_{bn} changes as the ring oscillator

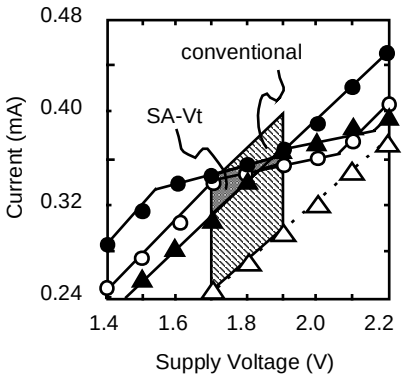
Table 1. Threshold voltages of test circuits.

	A	B	C	D
conventinal		○	▲	△
high-speed	●	○	▲	
pMOS (V)	-0.41	-0.47	-0.53	-0.88
nMOS (V)	-0.14	0.3	0.35	0.37

Vth @ Ids=10nA, W=15μm



(a) Operating speed.



(b) Power consumption

Figure 9. Measured operating frequency and current of the ring oscillator used as a test circuit controlled by SA-Vt CMOS.

keeps a constant frequency at 73 MHz. Four kinds of V_{th} samples were prepared for the experiments. (Their V_{th} values are shown in Table 1.) Samples B, C and D represent conventional circuits, while samples A, B and C represent high-speed circuits. Figure 9 shows the operating frequency and running current of the ring oscillator as functions of the supply voltage. When the supply voltage changes from 1.7 V to 1.9 V, the frequency and current varies within the hatched area in the conventional cases and within the shaded area in the high-speed case with the SA-Vt control. In the latter case, the worst frequency improved from 20 MHz to 55 MHz, the frequency fluctuation decreased from 44% to 15%, while the maximum current decreased from 0.40 mA to 0.37 mA.

Conclusion

Our proposed SA-Vt CMOS scheme keeps the delay of circuits constant by controlling the substrate bias. It compensates the fluctuation of CMOS devices from 44 to 15%, and increases the operating speed of CMOS circuits from 20 MHz to 55 MHz under worst-case conditions, without exceeding the power dissipation limit.

Acknowledgments

We wish to thank Hisayuki Higuchi, Takeo Shiba, Kenji Shiozawa, Shuji Ikeda and Katsuro Sasaki for their helpful discussions and the sample preparation.

References

[1] T. Kuroda, T. Fujita, S. Mita, T. Nagamatu, S. Yoshioka, F. Sano, M. Norishima, M. Murota, M. Kako, M. Kinugawa, M. Kakumu, T. Sakurai, "A 0.9-V 150-MHz 10-mW 4-mm^2 2-D Discrete Cosine Transform Core Processor with Variable-Threshold-Voltage Scheme," *1996 ISSCC Digest of Technical Papers*, pp.166-167, Feb. (1996).

[2] J. B. Burr, J. Shott, "A 200mV Self-Testing Encoder / Decoder using Stanford Ultra-Low-Power CMOS," *1994 ISSCC Digest of Technical Papers*, pp.84-85, Feb. (1994).