Low Power and Low Voltage CMOS Digital Circuit Techniques

Christer Svensson
Linkoping University
581 83 Linköping, Sweden
+46 13 281223
chs@ifm.liu.se

Atila Alvandpour
Linkoping University
581 83 Linköping, Sweden
+46 13 288965
atial@ifm.liu.se

1. ABSTRACT

One of many important factors affecting power consumption is the choice of circuit technique for logic, latches and flip-flops. We analyze the power consumption at circuit level and use the results to guide the choice of circuit technique. Several types of latches and flip-flops are compared regarding power consumption and speed. Comparing logic clearly indicates that simple static logic in general have the lowest power consumption. Another very important factor affecting power consumption is the supply voltage. We discuss the effect of low supply voltage on the choice of circuit technique.

1.1 Keywords

Low Power, Low voltage, CMOS, Digital circuits.

2. INTRODUCTION

Power consumption has became one of the major issues in electronic research since about 1990. Even if CMOS originally was considered a low power technique, down-scaling of the technology and new applications made power consumption a critical issue. It was early recognized, that nearly all aspects of system design affected power consumption, from the choice of fabrication process to the software to be run on the system. Old alternatives to logic design, as selftimed circuits, was now proposed for low power and completely new circuit techniques, as adiabatic circuits, was invented. In the present paper we will limit ourselves to power consumption aspects on conventional, nonadiabatic, synchronous CMOS circuit techniques.

One of several important factors affecting power consumption is the choice of circuit technique for logic, drivers, latches and flip-flops [1]. A good understanding of how the power consumption occur in the circuits is essential, and can be used to direct the search for more efficient circuits. We will therefore start with an analysis of the power consumption below, and then compare different circuit techniques. It must be recognized that comparisons always must be done with great care as context, process, layout style, data activity etc. strongly affects the results.

Another very important factor is the supply voltage, which strongly controls the power consumption, but also the speed. Trading speed for low power by voltage scaling is a very useful method to reduce power consumption [2]. An alternative is to reoptimize the fabrication process for lower supply voltage [3], optimizing process voltage and speed. In such new processes, also the threshold voltage is an important parameter. In these cases, the choice of circuit technique is again crucial. By choosing a fast circuit technique, for example, we may "pay less" speed for the low power. Low supply voltages, and possibly low threshold voltages may deteriorate the robustness of the logic, which needs to be counteracted by a proper choice of circuit technique.

3. POWER CONSUMPTION IN CMOS.

The power consumption of digital CMOS circuits is normally divided into three parts, dynamic, P_d, short circuit, P_{sc}, and static, P_s, power consumption [1,2]:

$$P = P_d + P_{sc} + P_s$$

The dynamic power consumption normally dominate, and is related to a node capacitor (for example the output capacitance of a simple gate) which is charged and discharged:

$$P_d = \alpha f_c C V_{dd}^2$$

where α is the signal activity of the actual node (probability for the signal to charge/discharge the capacitor during the clock cycle), f_c is the clock frequency and V_{dd} is the supply voltage. Let us consider the meaning of these parameters. The activity may be quite different on different nodes in the system [1]. The highest activity is normally on clocked nodes, with α=1 (clock cycles each cycle). Clock signals are therefore very important for power consumption. Next is normally precharged nodes in precharged logic. Such nodes have α=0.5, as they take a fixed value each half clock cycle, starting from a data value with equal probability of zero or one. Data, finally, may have different activity depending on their nature. Random data have an activity of 0.25, whereas real data normally vary between 0.01 and 0.25.

The clock frequency is trivial, it is set by the computing requirement. Capacitance should obviously be made as small as possible, specially on nodes with large activity. The effective capacitance is further discussed below. Supply voltage should be as small as possible, but is limited by speed requirements, as mentioned in the introduction (maximum frequency is reduced by lower V_{dd}-V_T, where V_T is the threshold voltage).

The short circuit power consumption is often described by the following expression, although it is not at all accurate [1]:

$$P_{sc} = (\beta/12)(V_{dd}-2V_T)^3(\tau/T)$$

where β is the symmetrical transistor gain factor, τ is input rise or fall time and T is the average time between transitions. The short circuit power is normally 10-20% of the dynamic power for a well designed circuit. It may however be considerably larger, even more than 100% of P_d, for cases with a slow input (large τ) and small load capacitance [4].

The average static power consumption of a CMOS circuit can be expressed as [1]:

$$P_s = (I_{d0n}+I_{d0p})V_{dd}/2$$

where I_{d0n} and I_{d0p} are the leakage currents of the n and p-transistors (or transistor blocks) respectively. These are normally very small, but depends strongly on V_T, $I_{d0} \sim \exp(-V_T/nV_{th})$, where n is about 1.5 and V_{th} is the thermal voltage (25 mV at room temperature). Therefore, when we start to decrease V_T, in connection to low supply voltages, the static power consumption becomes important and will in practice set a lower bound for V_T [3,5]. In some cases we use other circuit techniques than "pure" CMOS, as pseudo-NMOS or analog amplifiers, which circuits normally consume DC supply current and therefore have a large (dominating) static power consumption.

Let us finally discuss the capacitances in the circuits. For an inverter, the node capacitance is just the capacitive load at the output. This capacitance consists of the output capacitance of the inverter itself (drain-substrate and drain-supply capacitance and capacitances between wires and AC ground), input capacitances of the loading gates (mainly gate capacitances of the gates driven by the inverter) and capacitance of the wires connected to the output. For more complicated circuits, as a simple CMOS gate, the capacitance to use is the switched capacitance. This may depend on input data, as some nodes, for example between serial transistors, only switch for certain input values. Therefore, it is not very easy to estimate the power consumption for a given cell, rather we can give an average value [1] or we need to model it as data dependent. Internally in a gate or a cell, the transistor capacitances are normally dominating. Externally, that is for cases with relatively distant cells, wires normally dominates.

An additional problem is the capacitances not connected to AC ground, normally connected between input and output of a gate (for example the gate-drain capacitances), often referred to as Miller capacitance. This capacitance will occur on both the input and the output of the gate, with a value of about twice its physical value (as the voltage change of the capacitor is $+V_{dd}$ to $-V_{dd}$ upon switching) [1]. A more careful analysis indicate that the "amplification" factor is 1.8-2 [6]. The total effect on power will thus be nearly 4 times the capacitance value, making Miller capacitance very important inside cells.

From this short discussion we may make a few conclusions concerning circuit technique for low power consumption. Clocked nodes should be minimized in number and capacitance. Precharge should be avoided or minimized. Total capacitance should be minimized (minimum number of transistors, minimum wire lengths). This often means that minimum transistors should be used in logic and flip-flops, whereas driving strength is achieved by buffers, when needed. Signal slopes should be short.

4. DRIVERS

A very important element in a design is the driver. It is well known that a minimum delay driver consists of a tapered inverter chain, with a tapering factor f around 3. The switched capacitance of such a driver is [1]:

$$C = (1+C_0/C_i)(1-2C_i/C_L)C_L/(f-1)$$

where C_i and C_0 is the minimum inverter input and output capacitances respectively and C_L is the load capacitance. For large C_L and with f = 3 and $C_0/C_i = 1$, C is about equal to C_L, meaning that the driver consumes as much power as its load. This is often unacceptable, why we should use larger values of the tapering factor in low power designs. We may use f of up to, say, 9 with a very limited speed loss. As the largest single load in a circuit normally is the clock, the driver capacitance will strongly affect the clock power consumption and thus further emphasize the importance of small clock loads.

5. LATCHES AND FLIP-FLOPS

Latches and flip-flops are important elements in synchronous logic, often controlling speed and robustness of a design. Many different circuits solutions exists, static and dynamic, single ended or differential. Let us choose a limited number of existing solutions for a comparison and then discuss the results. As noted above, comparisons are very tricky, so we will compare a set of circuits designed in the same process using the same design style and then simulated in the same simulator [7]. The circuits chosen and the power consumptions and delays are shown in Figs 1 and 2. In both figures the bar gives the power consumption for data activities from 0 to 0.5 and the circle corresponds to an activity of 0.25. For details, see [7].

Fig. 1 shows the results from some dynamic latches. The latches are, from the left, “Classic” (inverter followed by transmission gate), NPTSPC (Non-precharged True Single

Phase Clocked), C^2MOS, Precharged TSPC, DSTC [9], CVSL, p-CVSL, and p-DSTC. All are of n-type, except the ones with prefix p. First we may note that it is quite possible

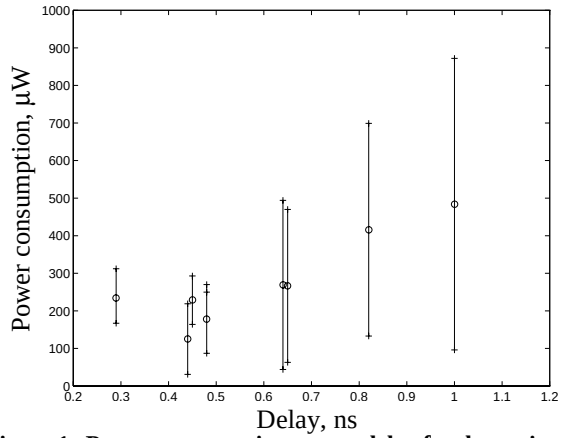

Figure 1. Power consumption versus delay for dynamic latches

to combine low power consumption and short delay in the same circuit. This is of course very valuable, but also understandable. Simplicity and low transistor count leads to both low power and short delay. The latch with the lowest power consumption is the non-precharged TSPC latch NPTSPC), also used in the first Alpha processor. It is worth noting, that a very early technique for low power dividers was based on a technique very similar to TSPC [8]. The fastest latch is the "Classic" one, with somewhat larger power consumption.

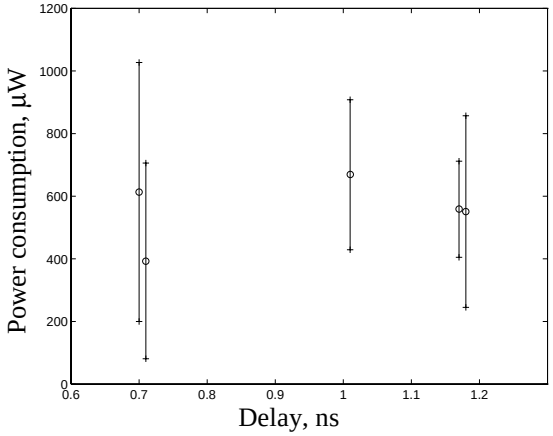

Figure 2. Power consumption versus delay for static flip-flops.

Fig. 2 shows some static flip-flops. The flip-flops are, from the left, RAM-type (six-transistor RAM-cell with two data input transistors), SSTC [9], transmission-gate based, combinatorial gate based and STSL [10]. Here, the recently proposed SSTC flip-flop [9] has the least power consumption and also close to the least delay. The key here is the few clocked transistors used (only 2 for the full flip-flop). Traditional flip-flops, based on transition gates or combinatorial gates are considerably slower at larger power consumption, as is the STSL flip-flop used in the "low power" StrongARM processor [10].

6. LOGIC

Logic circuit styles is even harder to compare than latches and flip-flops. In this case not only context, layout style, process etc. is important, but also the logical function to be realized [11]. It is therefore even more important to perform complete designs of many different logic functions using the same layout style, process etc., in order to compare different logical styles. Unfortunately, very few comparisons of this type is published, but one will be discussed below.

Initially, we can try some general considerations. We did some rough estimates of power consumption of simple gates, based on activity and estimated transistor capacitances [1]. From these comparisons we concluded that plain static CMOS consumes least power. Precharged logic consumes a lot of power because of the unnecessary activity and clocking, also discussed above. Differential logic, as complementary pass transistor logic or CVSL also consume more power than static CMOS in our comparison, although the difference is not large enough to make the comparison reliable. In fact many recent papers claim that pass transistor logic gives rise to less power consumption than static logic [12].

A more careful comparison between static CMOS logic and complementary pass transistor logic (CPL) demonstrates that CPL is preferable for certain functions, as exor and therefore adders, but static CMOS is superior in all other cases [11]. When comparing larger designs (more complete functions), static CMOS seems superior. One example of an buffered parallel-prefix 32-bit adder, designed in static CMOS and in CPL is shown in Table 1 [11]. Here, the speed

	Delay	Power
Static CMOS	4.14 ns	7.5 mW
CPL	3.47 ns	25.9 mW

Table 1: 32 bit adder in 0.5 µm CMOS at 100 MHz.

is somewhat better for CPL, but the power consumption very large.

7. LOW SUPPLY VOLTAGE

Low supply voltage is a very important route for low power [2,3]. As speed is reduced approximately as $(V_{dd}-V_T)^{-1}$, we need to counteract the speed reduction. This can be done by using high speed circuitry (which is faster from the beginning) and by reducing the threshold voltage. It should be noted that the speed dependence on supply voltage leads to an increased sensitivity to threshold voltage variations when V_{dd} is close to V_T.

The trend towards lower supply voltage will introduce new

demands on the circuit techniques. First, the circuits must behave well at reduced supply voltage, and keep their speed and robustness as well as possible. Second, they should preferably also behave well at reduced threshold voltage, facilitating the exploitation of very low V_{dd} and V_T. Third, timing robustness must probably be improved in low V_T processes, in order to accept a larger spread in delay caused by fabrication process induced spread in V_T. Concerning these points, we have made some preliminary simulations to verify the voltage scalability of different circuit techniques.

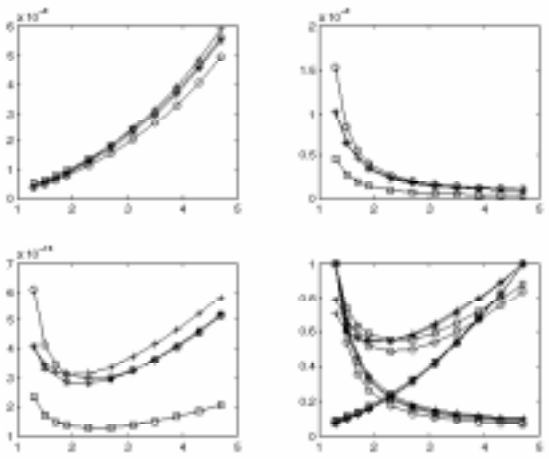

Figure 3. Power consumption, delay, power-delay product and normalized values versus supply voltage.

In Fig. 3 we show the power consumption, delay, power delay product and normalized values of these versus supply voltage for some flip-flops in a 0.8 µm process with V_T of about 0.8 V. The flip-flops are transmission gate type with trickle inverters (circles), full transmission gate flip-flop (asterisks), combinatorial gate type (crosses) and SSTC [9] (squares). What we can see is that all flip-flops behave very well down to supply voltages quite close to V_T, and that they behave very similarly (seen in the normalized plot). All basic CMOS circuits therefore seems well suited for voltage reduction. Some further simulations on the same process, also indicates that these flip-flops behave well for the simultaneous reduction of V_T and V_{dd}, down to $V_T = 0$ and $V_{dd} = 0.9$ V.

8. CONCLUSIONS

We have discussed the power consumption of conventional CMOS circuit techniques. Low power consumption is achieved by few and minimum sized transistors, limited clocking, avoidance of precharge and fast slopes. Several types of latches and flip-flops was compared regarding power consumption and speed. We found that it is possible to choose latches and flip-flops which combine low power consumption and high speed, for example dynamic latches based on inverter-transmission gate or nonprecharged TSPC, or static flip-flops based on the RAM-cell with few clocked transistors. Comparing logic clearly indicates that simple static logic in general have the lowest power consumption. Pass transistor logic is superior for some special cases, as for example the exor function. Another very important factor affecting power consumption is the supply voltage. We discuss the effect of low supply voltage on the choice of circuit technique and conclude that robust circuits should be chosen. Commonly used latches and flip-flops is shown to behave well also at very low supply voltages.

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