TUTORIAL 4
INTERCONNECT IN HIGH SPEED DESIGNS:
PROBLEMS, METHODOLOGIES AND TOOLS

Speakers:

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Background: This tutorial is intended to help circuit designers and CAD tools developers gain an understanding of the problems, the existing tools, and the critical CAD needs in the area of interconnect for high speed systems.

Description: This tutorial will begin with a designer’s perspective on using existing design strategies, topologies, and tools to optimize high speed designs. In particular, the example of designing clock distribution networks in high-end VLSI processors will be examined in detail. The impact of on-chip transmission line effects will be demonstrated, and some of the difficulties of managing those effects will be described.

The second part of this tutorial will focus on the current state of extraction techniques for on-chip interconnect. The problems of extracting resistance, capacitance and inductance will be described, followed by a description of the currently available techniques. The advantages and limitations of formula-based approaches and the various styles of recently developed fast 3-D analysis techniques will be discussed.

The third part of this tutorial will focus on the problem of generating simplified circuit models from the results of extraction. Many of the reduction techniques based on moment-matching will be examined and compared, with a focus on issues such as robustness, accuracy and passivity. The interaction between reduction approaches and extraction algorithms will be discussed, and the impact of the need for on-the-fly reduction examined.

Phillip J. Restle received a B.A. in Physics from Oberlin College in 1975, and a Ph.D. in physics from the University of Illinois at Urbana in 1986. He then joined the IBM T. J. Watson Research Center where he has worked on CMOS device and DRAM testing and since 1993, developing tools and designs for VLSI clock distribution networks.

Joel Phillips received his PhD in Electrical Engineering and Computer Science from MIT in 1997 and is now with the mixed-signal group of Cadence Design Systems. His work has been in numerical techniques for simulation and modelling of electronic circuits.

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