TUTORIAL 3
HIGH-LEVEL DESIGN VALIDATION AND TEST

Speakers:

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Background: This tutorial is intended for designers, CAD tool developers, and researchers interested in addressing verification and test of VLSI systems at higher levels of abstraction, including verification and test of processors, general ASICs, and hardware-software system chips.

Description: To meet aggressive design cycle, complexity, and productivity requirements, more electronic systems than before are being specified and designed at higher levels of abstraction, involve embedded processors and other programmable components, and achieve design re-use with hardware and software components. In order not to compromise the productivity gains obtained by component-based systems, verification and test should be addressed early in the design cycle. This tutorial addresses the challenges, proposed methodologies, and current industrial practices in verification and test of components and component-based systems at higher levels of abstraction.

The first part of the tutorial will address validation of components like processors at the register-transfer and higher levels. Techniques currently used for validation based on simulation as well as formal approaches will be described. Abstractions for reducing the design exploration space will be discussed, with applications to providing coverage measures for functional simulation vectors, coverage-directed test case generation and checking for correctness of properties.

Next, system-level validation will be addressed, including validation of hardware-software embedded systems. Validation at various levels of the design hierarchy will be considered, including algorithmic, bus-functional, and architectural levels. Simulation and validation models, like HDL models, instruction-set simulation models, bus-functional models, and full-timing models will be described. Validation methodologies currently used to verify the correctness of such systems will be described, including emulation, in-circuit emulation, compliance test environments, instruction-set simulation, and hardware-software co-simulation.

Finally, the tutorial will address system-level testing issues, with emphasis on testing component-based system chips. It will discuss test access and isolation mechanisms of the embedded components, and silicon debug and diagnosis. Current practices in testability schemes, such as BIST and scan, for embedded cores will be addressed. Finally it will discuss the recent challenges and adopted strategies to implement an integrated test strategy from embedded components to systems.

Sujit Dey, University of California at San Diego, La Jolla, CA, is an associate professor of Electrical and Computer Engineering. His research activities include CAD tools for high level design and test, and design, validation, and test of hardware-software system chips. He was a Senior Researcher at NEC, Princeton, NJ.

Jacob Abraham, University of Texas, Austin, TX, is a professor of Electrical and Computer Engineering and Computer Sciences, and Cockrell Family Regents Chair in Engineering. He received his Ph.D. from Stanford University in 1974. His research interests include test, verification and fault tolerance.

Yervant Zorian, LogicVision, Inc., San Jose, CA, is Chief Technology Advisor. His responsibilities include research and consulting in the areas of embedded core, IC and multi-chip module self-testing. He was a Distinguished Member of Technical Staff at Lucent Bell Laboratories, Princeton, NJ.