NOVEL SIMPLE MODELS
OF CML PROPAGATION DELAY

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Abstract

Accurate and simple models of CML propagation delay are
given. The approach used is new. The propagation delay is
represented with a few terms, providing a better insight into the
relationship between delay and its electrical parameters, which
in turn are related to process parameters. The most accurate
model has a typical and worst case errors as low as 2% and
5%, respectively.

I. INTRODUCTION

Recent advances in optical communication demand very high-
speed circuits such as multiplexing, demultiplexing, threshold
detection, etc. [1]-[9]. The current mode logic (CML) is a
fundamental gate of bipolar high-speed circuit.

In the design and analysis of this bipolar digital circuits, estima-
tion of the propagation delay is a fundamental step. The
propagation delay can be obtained by Spice simulations.
However, a circuit optimization procedure based on Spice
simulations requires a very large number of simulation runs.
Moreover, the use of Spice like simulators for large circuits is
impractical. Thus, the development of accurate and efficient
delay models is needed.

Various different approaches have been proposed in the
literature to determine the delay expression of CML circuits.
Those based on sensitivity analysis has many terms and hence
are not useful for a first paper and pencil design [10]-[12].
Moreover, in order to evaluate the coefficients used in the
model many simulations are needed. Other approaches are
based on linearization of the device models [14]-[17], or on
average branch current analysis [18]-[19], but they are complex
to use during design or not sufficiently accurate.

Fig. 1. CML gate

In this communication we give accurate and simple models of
CML propagation delay. The approach used is new. The models
starts from the small signal model properly evaluated. The high-
speed feature of CML is due to its behaviour in the linear
region.

The propagation delay is represented with a few terms,
providing a better insight into the relationship between delay
and its electrical parameters, which in turn are related to
process parameters. Moreover, high accuracy is achieved by
introducing coefficients which minimize the error between
analytical and simulated results. This improved mode,
differently from that obtained with the sensitivity analysis, only
needs five Spice simulations.

In order to validate the models, a comparison using both a
traditional and a high-speed bipolar process was carried out
under many bias conditions and output loads. For both
II) SIMPLE PROPAGATION DELAY MODEL

A CML gate is shown in Fig. 1. In order to achieve high-speed performance its transistors work in a linear region and can be represented with a linearized model which is topologically equal to the Spice small signal model. Moreover, since the circuit is symmetrical and differential operation is assumed, we can limit our analysis to the half circuit model in Fig. 2. The transconductance, \( g_m \), and input resistance, \( r_m \), are those of the small signal model \( l/2V_T \), and \( 2\beta IPV_Tl/\), respectively, and the resistances \( r_b \), \( r_e \), and \( r_C \) are resistive parasitic. However, since voltages move rapidly over a wide range, unlike the traditional small signal model, we have to properly evaluate the capacitances following the procedure shown in [20]. More specifically, the junction capacitances, \( C_j \), are those in a zero-bias condition, \( C_{jc0} \), multiplied by a coefficient \( K_j \) given by

\[
K_j = \frac{(\phi - V_1)^{1-m} - (\phi - V_2)^{1-m}}{1-m} \left[ \frac{V_2 - V_1}{1 - m} \right] 
\]

where \( \phi \) is the built-in potential across the junction, \( m \) is the grading coefficient of the junction, and \( V_1 \) and \( V_2 \) are the minimum and maximum direct voltages across the junction, respectively. Moreover, to take into account the distributed effect of the base-collector capacitance, \( C_{bc} \), we have split it into an intrinsic, \( C_{bc} = X_{cje}X_{bc} \), and extrinsic, \( C_{bcx} = (1 - X_{cje})C_{bc} \), part, via the technological parameter \( X_{cje} \) which ranges between [0-1]. The diffusion capacitance is \( C_D = 2r_F/C_{bc} \), where \( r_F \) is the transistor transit time [10]. Thus the base-emitter capacitance, \( C_{be} \), is equal to the diffusion capacitance, \( C_D \), plus the base-emitter junction capacitance, \( C_{je} \). (i.e., \( C_{be} = C_D + C_{je} \)).

Assuming a dominant pole behaviour with a time constant, \( \tau \), the propagation delay, \( \tau_{PD} \), is equal to 0.69\( \tau \). Thus, after simple approximations in which we neglect the term \( r_m \), we get

\[
\tau_{PD} = 0.69 \left[ \frac{r_f + r_b}{1 + g_m r_F} + C_{be} \left( 1 + \frac{g_m r_b}{1 + g_m r_F} \right) + \right. \\
\left. + \left( R_e + R_C \right) \left( C_{be} + C_{bc} + C_{cj} + R_e C_e \right) \right] 
\]

(2)

The propagation delay is the sum of four main terms which have a simple circuit meaning. Indeed, these four terms can be evaluated with pencil and paper. The first term is the contribution made by the base-emitter capacitance, the second is made by the Miller effect on the intrinsic base-collector capacitance, the third is a contribution which arises at the inner collector node (i.e., before parasitic resistance \( r_e \)) and the last one is due to load capacitance at the output node. It is worth noting that the term \( g_m/(1 + g_m r_F) \) is the equivalent transconductance of the transistor having a resistance \( r_e \) at the emitter node.

Validation results

In order to evaluate the accuracy of the simple model, a comparison between the propagation delay given by (2) and Spice simulations was carried out. Moreover, to generalize the comparison, two different technologies were taken into consideration. The first is a BiCMOS technology whose npn bipolar transistor has a transition frequency equal to 6 GHz, the second is a high-speed bipolar technology with only npn transistor with a transition frequency equal to 20 GHz.

The circuits have a 5-V power supply and a 250-mV logic swing which determines the junction capacitances reported in Table I and Table II for the 6 GHz and 20 GHz transistors, respectively. Table I and Table II also include the minimum and maximum direct voltages across the junction, the built-in potential, the grading coefficient, the zero-bias capacitance and the resulting \( K \).

The error found versus bias current \( I_{SS} \) and with a load capacitance \( C_L \) equal to 0, 100F and 1pF, is plotted in Figs. 3 and 4 for the 6 GHz and 20 GHz transistor, respectively. Its worst case is 18% and 42%, respectively. Moreover, outside the high-level injection region, which is for bias current higher than 1.4 mA and 2.4 mA for the 6 GHz and 20 GHz, respectively, we get a mean error equal to 5% and 17%, respectively.

The error reduces increasing the load capacitance. This is because the contribution due to the linear capacitance \( C_L \) becomes dominant. Finally, it is worth noting that although results for high-level injection bias currents are less significant, the errors are still low.
(r_e + R_C) \left( K_{nt} X_{nt} C_{nt} + K_{nct} (1 - X_{nt}) C_{nt} + K_{nct} C_{nt} \right) \\

Of the many ways to obtain the coefficient $K$ the most efficient is that of minimizing the functional below, since it requires few simulation runs.

$$S(K_{nct}, K_{nt}, K_{nt}, K_{nt}, K_{n}) = \sum_{j=1}^{n} \frac{\tau_{PDSS} (I_{SSj}) - \tau_{PD} (I_{SSj})}{\tau_{PDSS} (I_{SSj})}$$

(4)

In (4), parameter $n$ is itself a variable, but, according to our experience, it is set to 5. Simulations differ only for bias current value, because we consider the load capacitance in the worst condition (i.e., $C_L=0$). Minimization of functional $S$ is achieved with a numerical software such as Mathcad, Matlab, etc..

**Validation results**

The set of current values used to minimize functional (7) are [0.1 mA, 0.2 mA, 0.6 mA, 1 mA, 1.4 mA] and [0.1 mA, 0.4 mA, 1.2 mA, 1.6 mA, 2.2 mA] for the 6 GHz and 20 GHz technology, respectively. The coefficients $K$ obtained are reported in Table III for both technologies.

The error found versus bias current $I_{SS}$ and with a load capacitance of 0, 1000F and 1pF, is plotted in Figs. 5 and 6 for the 6 GHz and 20 GHz, respectively. It is worth noting that there is no difference in the accuracy of the model between the two technologies. The worst case is lower than 5% for both of them, and outside the high-level injection region, we get a mean error lower than 2%.

**III) ACCURATE PROPAGATION DELAY MODEL**

Although the accuracy of the previous model may be adequate during the design step of a CML, it is not sufficient to implement a simulation model to evaluate the delay of a complex system. We thus have to improve accuracy of the model. The strategy adopted was that of using (5) and evaluating the capacitance coefficients from a few simulation runs by means of a numerical procedure. More specifically, representing each junction capacitance with its zero-bias value and introducing a corrective coefficient for each capacitance, from (5) we get

$$\tau_{PD} = 0.69 \left( \frac{r_e + R_C}{1 + g_m r_e} \left( K_{nt} C_{nt} + K_{nct} C_{nt} + K_{nct} C_{nt} \right) + 
\right.$$

$$t_0 K_{nct} X_{nt} C_{nt} \left( \frac{1 + g_m r_e}{1 + g_m r_e} \right) + R_C C_L +$$

(3)
REFERENCES


### TABLE I

<table>
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<tr>
<th>Capacitance</th>
<th>V₁</th>
<th>V₂</th>
<th>φ</th>
<th>m</th>
<th>C₁₀</th>
<th>K</th>
<th>Resulting C₁</th>
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<td>C&lt;sub&gt;bce&lt;/sub&gt;</td>
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<td>250 mV</td>
<td>0.646 V</td>
<td>0.35</td>
<td>27 fF</td>
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<tr>
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* X<sub>CJC</sub>=0.146
+ I<sub>S</sub>=8.91E-18 A

### TABLE II

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* X<sub>CJC</sub>=0.23
+ I<sub>S</sub>=7.4E-18 A

### TABLE III

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