Design Issues of LC Tuned Oscillators for Integrated Transceivers

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Abstract

VCO for wireless receivers must fulfill tight requirements of phase noise and their complete integration in silicon VLSI technologies is still an open issue due to the low quality factor of the inductors. In this paper we address some of the constraints met in the design of low noise oscillator stages: the tank topology and its quality factor, the dynamics of the transconductor stage and its loading effects, the limitation resulting from the AM-to-PM conversion.

I - Introduction

Specifications of GSM standard put severe requirements on the stages constituting the whole receiver, and in particular onto the phase noise characteristics of the internal synthesizer. For instance a phase noise of -140 dBc/Hz at 3 MHz (see Ref. [1]) from the carrier is needed to meet the tightest blocking request. This figure has not been matched so far by ring oscillators, either bipolar or CMOS. In fact Ref: [2], [3] demonstrate -88 dBc/Hz at 4 MHz and -105 dBc/Hz at 5 MHz respectively. LC tuned oscillators can achieve this performance but only with external inductors. Recently some promising implementations of integrated inductors have been proposed (see for example [4], [5], [6] and [7]), opening new perspectives for the design of fully integrated solutions.

II - A glimpse at noise analysis of VCOs

Fig. 1 shows the schematic structure of an LC tuned oscillator:

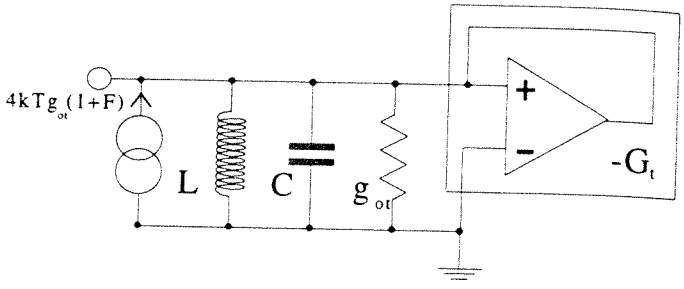

Fig. 1 - Schematic structure of an LC tuned oscillator

where g_{ot} represents the overall losses, $-G_t$ is the negative transconductance given by the active element connected in positive feedback, and $4kTg_{ot}(1+F)$ is the equivalent current noise generator in parallel to the tank.

The term $4kTg_{ot}$ comes from the loss conductance g_{ot}, whereas $4kTg_{ot}F$ counts for the noise of the transconductor characterized by a suitable noise factor F. Taking α as the offset from the angular frequency ω_0 of the carrier, and $A_0^2/2$ as the carrier power, the Single Sideband to Carrier Ratio can be written as:

$$SSCR(\alpha) = \frac{1}{2}\cdot\frac{4kTg_{ot}\cdot(1+F)}{A_0^2/2}\cdot\frac{1}{(2\alpha C)^2} = \\ = \frac{1}{2}\cdot\frac{1}{A_0^2/2}\cdot\frac{kT}{C}\cdot\frac{\omega_0}{Q}\cdot\frac{1}{\alpha^2}\cdot(1+F) \qquad (1)$$

where we used $\omega_0/Q = g_{ot}/C$. Since g_{ot} represents the overall losses, that is including also the contribution of the active element, Q refers to the whole system and not only to the tank. The term $1/(2\alpha C)^2$ is the noise shaping due to the LC tank, and the leading factor 1/2 takes into account that half of the current noise power gives rise to phase noise. The above equation highlights that low SSCR values require the increase of both A_0 and Q.

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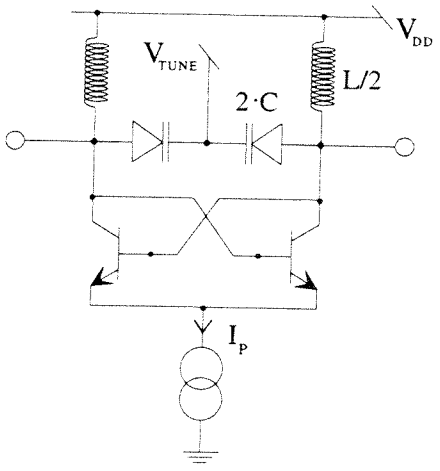

Fig. 2 - A practical realization of the oscillator in Fig.1

Fig.2 shows a typical realization of VCO schematic sketched in Fig.1. The structure is fully differential: the tank is symmetrical, with varactor diodes employed to tune the oscillation (angular) frequency $\omega_0=1/(LC)^{1/2}$. The output waveform is then taken as the difference between the two collector voltage signals. The bipolar crossed couple implements the active element in positive feedback, giving $-G_t = -g_m/2$, where g_m is the transconductance of a single transistor.

By increasing the bias current I_P, the transconductance of devices and therefore the oscillation amplitude increase. Usually to maximize the amplitude (see SSCR expression) the tail current is raised until the stage is driven to operate in hard-switching regime, that is one transistor of the pair is alternatively off, while the other one is biased with the full I_P. The non-linear mechanism setting the oscillation amplitude is provided by the saturation of base-collector junctions of BJT's. The same effect happens in a CMOS circuit and in this case it is named de-saturation.

Based on Eq.(1) let us now consider what kind of specifications are needed to meet -140 dBc/Hz at 3 MHz. Even if the active element are noiseless, i.e. F = 0, at ω_0=1.8 GHz a Q factor of about 30 is needed if the oscillation amplitude A_0 is about 400 mV. The Q request is relaxed if A_0 = 900 mV. In this case the Q must be about 10. Nowadays Q values of 30 can be achieved only by using external inductors, while integrated inductors can reach values of the order of 10. The example highlights that the only chance to meet low noise performance with fully integrated VCO is to increase the oscillation amplitude, driving the transconductor in hard-limiting regime, otherwise prohibitive values of Q can be necessary.
Regarding the value of the noise factor F, it should be noted that when the transconductor operated in hard non-linear regime its evaluation is not trivial. A detailed discussion of this topic may be found in Ref. [8]. To the purpose of the present paper we remind that the main noise sources of the bipolar stage working in non-linear regime are: the Johnson contribution from the spreading resistance $r_{bb'}$ and the noise from the tail generator S_{IP}. The latter being unexpected if the noise analysis is performed following the usual linear theory. The contribution due to the tail noise can be minimized by accurate design of the steady current generator, while the noise due to spreading resistors can be reduced by connecting more transistors in shunt configuration. As the noise of the transconductor stage is properly minimized F is usually not larger than 3. Therefore the key issues of the circuit design remain to increase A_0 and not to degrade the Q. Some of the problems that must be faced to fulfill this task are discussed in the following.

III - The tank

Usually the highest losses come from the two tank elements, the inductor and the varactor. With discrete components high Q values are easily achieved, but landscape changes for integrated solutions: the varactor can reach a figure close to 30, while the Q factor of the inductor is limited to a value of 10-12, or even less (about 5) in VLSI CMOS technologies. However the most recent works (such as [4] and [5]) report inductor quality factors as high as 20 acting on both substrate resistivity and metal thickness and further enhancements are expected in the near future. While waiting for technological improvements a more complex tank structure has been proposed to circumvent the limitations of the integrated components. The so-called "crystal-like tank" in Fig.3 (see [9]) resembles the lumped-elements model of a crystal; the resonance frequency of the network is of course $1/(LC_S)^{1/2}$, where C_S is the series of C and C_1 and the losses represented by g_{ot} are only due to the capacitor C. The signal output is the one taken across C.

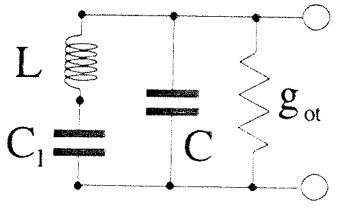

Fig. 3 - A crystal-like tank in which the only losses are due to capacitor C

Let us compare the tank of Fig.3 with the ones in Fig.1 and 2 at equal oscillation amplitude A_0. It can be

easy shown that the losses are the same in both cases, but in the crystal-like tank the energy stored is higher, since it depends on the voltage across the series of C and C_1 which is larger than the voltage amplitude at the tank output nodes. In other words the Q factor of the crystal-like tank is increased and a detailed calculation shows a corresponding reduction of the phase noise by a factor:

$$\left(C_1/(C+C_1)\right)^2 \qquad (3)$$

The smaller C_1 the larger the advantage of the latter configuration. However, it must be stressed that this result, proposed in Ref. [9], holds as long as the low-Q element is the integrated varactor; in this case a small integrated capacitor C_1 with negligible losses can be added in series to the inductor [10]. Instead if the element with the highest losses is the inductor the same type of improvement can be achieved by placing a larger inductor L_1 with a high Q factor, in series to the lossy inductor L and picking up the output signal across L. However, as long as all the inductors must be integrated, this solution is of no help.

IV - The transconductor cell

Let us now examine the active transconductor. As a first step the cell may be derived from one of the three basic transistor schemes: Colpitts, Hartley, LC tuned-collector [11]. In order to make possible a larger oscillation amplitude these single-transistor topologies may be transformed into differential stages. This result may be accomplished by joining a cell with a mirrored replica and placing resistors between the supply voltages and the nodes lying on the symmetry axis. These nodes are balanced with respect to a differential oscillation and the resistors do not affect the differential dynamics of the system, whereas they prevent any common mode oscillation [12].

As an alternative a differential stage may be adopted. Fig.4 shows two different solutions to improve oscillation dynamics of the basic stage in Fig.2. In Fig.4a the highpass $C_B R_B$ network uncouples the steady voltages of collector and base. The base voltage should be either:

- low enough to let a larger voltage swing between base and collector;
- high enough to avoid the saturation of the transistor of the tail generator.

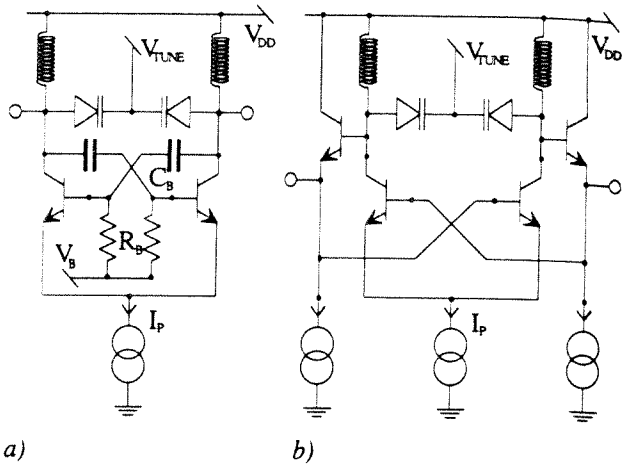

Fig.4 - Different solutions to increase the output amplitude: "highpass" uncoupling a) and voltage shift realized with the emitter followers b).

Taking $V_B \approx 1.3$ V the oscillation peak amplitude A_0 can reach near 2 V even with a voltage supply of 2.4 V.
In Fig.4b the voltage shift is instead obtained by the base-emitter voltage of a follower [13]. In this case the maximum A_0 can reach about 1.2 V.
As a final remark note that any fully differential structure working in hard switching regime loses the high rejection to supply noise.

The second point discussed here concerns the loading effect of the transconductor cell on the Q factor of the VCO. This effect has seldom been considered; on the contrary, cell losses must keep apace with technological improvement of the integrated tank, not to become in turn the main shortcoming.
In the differential stages so far discussed, there is a parasitic current which flows into the bases, which is inversely proportional to the impedance seen through them. At the oscillation frequency this impedance is not so high as one may expect. This statement also holds for a MOS stage. In fact, at the oscillation frequency the capacitors bypass the active devices (BJT or MOS) and the resistance seen on the emitter of these elements loads the tank. This effect is much similar to what happens in a simple emitter, or source, follower. Fig.5 sketches the frequency dependence of the input impedance of a follower with a resistor R_C on the collector. The first pole of the impedance lies near $f_\beta = f_T/\beta$; for the MOS transistor this value is zero, where the impedance Z_{IN} is infinite. At high frequencies all the capacitors are shorted and the impedance reduces to the parallel of R_E and R_C.

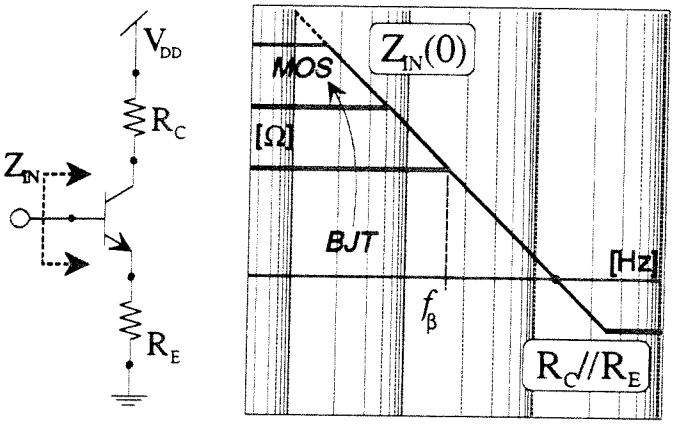

Fig.5 - Schematic plot of the impedance (magnitude) seen in the base of a bipolar or MOS transistor, as a function of the frequency

In silicon integrated VCOs always happens that

$$f_T/\beta < f_{osc} < f_T \qquad (4)$$

(generally f_{osc} is up to 3.6 GHz and f_T around 20 GHz) and therefore the base impedance at f_{osc} is still falling, and a non negligible parasitic current is drawn from the bases.

However the quantitative evaluation of the load effect of the oscillator cell is not easy, because the stage is switching, and the equivalent resistance on the emitter of the two transistors (R_E) is periodically varying. Referring to the circuit in Fig.4a:

- when the oscillation on the tank reaches a peak, one bipolar is on and the other off; thus the emitter of the former sees its Early resistance r_0 in parallel with the Early resistance of the tail; the base eventually shunts this value with R_B present in Fig. 4a;
- when the oscillation is at the zero-crossing , the stage is in balanced state and each emitter sees $1/g_m$ in the other device.

Moreover, at the oscillation frequency, the impedance load on each collector reduces instead to about $R_C=1/(2\cdot g_{ot})$.

The oscillator shown in Fig. 4a has been simulated with Cadence SPICE. Fig. 6a) reports the differential oscillation voltage when I_P = 10 mA and the total parasitic current (difference of the base currents) of the transconductor. The base currents are heavily anharmonic because of the large driving signal amplitude. Moreover since the frequency is very high a large amount of the current is a *reactive* component due to C_π and C_μ. Since we are looking for a parasitic contribution given by an equivalent *resistive* element, we have extracted only the component in phase with the driving signal. Since we are not dealing with sinusoidal waves we have:

- decomposed the current waveform in series of harmonics at multiples of f_{osc}
- found the component of every harmonic which is in phase with the driving voltage carrier
- reconstructed the "in-phase" parasitic current by superimposing all the contributions previously found.

Of course a sinusoid at $3\cdot f_0$ could not strictly be defined "in phase" nor "in quadrature" with a carrier at f_0, but the phase difference can be derived taking the nearest zero-crossings.

Fig.6b shows the extracted "in phase" current; note the difference between the vertical scales for the two currents. From the ratio between the voltage carrier and the corresponding parasitic current we compute the time-dependent values of the parasitic resistance R_{IN}. From Fig. 7 it can be noted to what extent the numerical results are close to the theoretical predictions: with a V_{EARLY} = 50 V (i.e., r_0 = 5 kΩ) and a R_B = 2 kΩ, the maxima of the curve should all be:

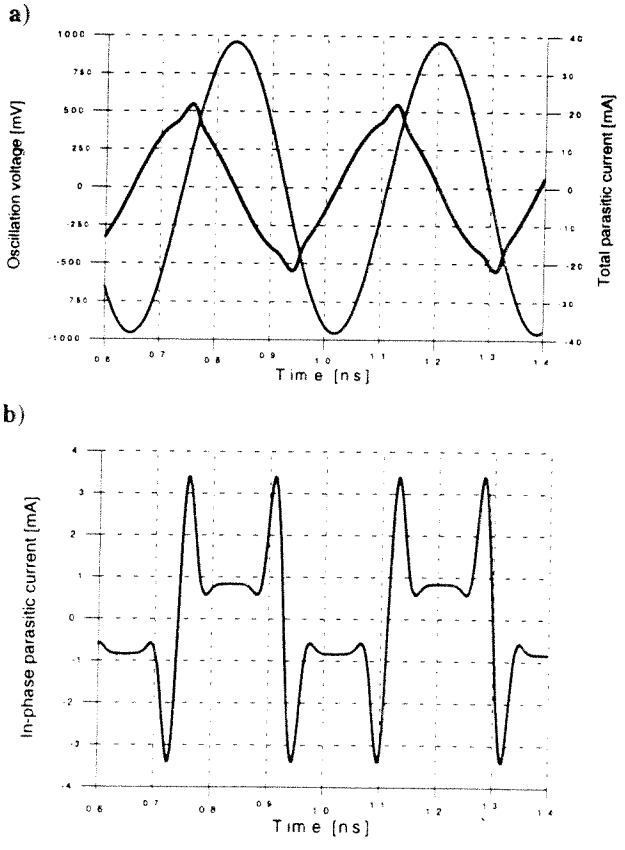

Fig. 6 - Oscillation amplitude and transconductor current a) and b) resistive component of this current

$$R_B // r_0 = 2k\Omega // 5\,k\Omega = 1.4\,k\Omega \qquad (5)$$

Since the quality factor Q is a parameter depending on the average behavior of the system, the Q_T of the cell

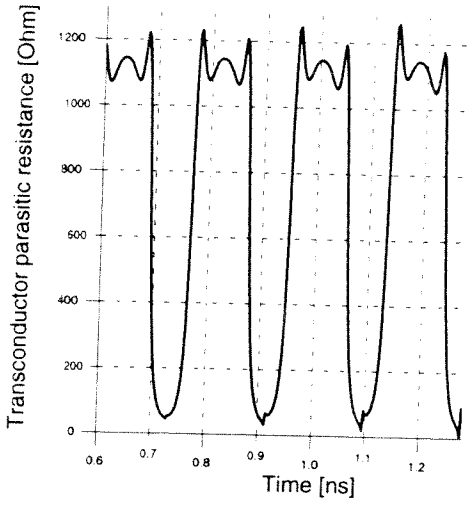

Fig.7 - Time varying value of the parasitic load resistance due to the transconductor

it should be computed by taking the mean value of R_{IN}; for the case proposed we get $\langle R_{IN} \rangle = 714\ \Omega$, and thus $Q_T = \omega_0 R_{IN} C = 30.5$. This value threatens to worsen the overall performance of the VCO, which is noticeably sensitive to even little variations of its quality factor. This implies that striving to enhance the quality factors of the passive components of the tank is of little worth if the transconductor stage shows such a losses, e.g. for high oscillation amplitudes.

Fig.8 shows the variation of the Q factor of the active cell with the bias current. It should also be remarked that as I_P is increased to attain larger A_0 values, high injection effects like β and Early resistance derating reduce the total impedance seen through the base and the C_π rise further degrades the f_T (see Fig.5). Similar considerations also apply to single-ended stages as well as to CMOS transconductors.

V - Low-frequency noise and the $K_{am/pm}$ problem

The request for high oscillation amplitude leads to large bias current; not only the noise of the bias source I_P increases but also another effect gains importance: AM-to-PM noise conversion.

The low frequency noise components coming from the tail reaches the tank by passing through the differential stage switching at ω_0, that therefore acts like a mixer. These components are thus upconverted in an amplitude modulation noise around the carrier and they can be theoretically filtered away by an hard limiter. The behavior of a practical realization is instead different. In fact varactors and other non-linear reactive elements are able to convert the AM noise into PM noise and it is then shaped by the loop, much like $(1/2)\,4kTg_{ot}$ (i.e. like the phase noise fraction of the thermal noise of g_{ot}) found in Eq.(1).

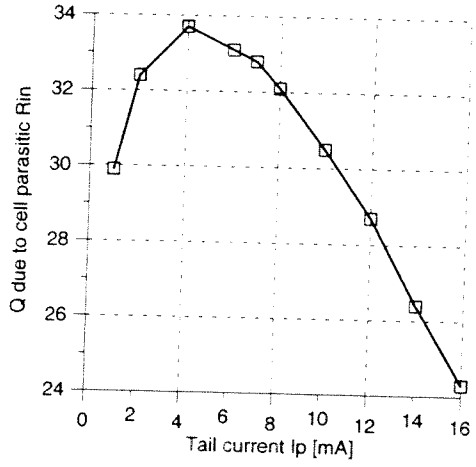

Fig.8 - Reduction of the quality factor of the cell; the effect is due to the reduction of the f_T

In order to better clarify the AM-to-PM conversion, let us consider the varactor behavior. An AM noise with a zero mean value determines a random variation of the capacitance value, around the one fixed by polarization. Since the reverse voltage-capacitance relation is non-linear, this noise causes a capacitance modulation with a non zero mean value and ultimately it moves the tank resonance frequency. This jitter of center frequency translates of course into phase noise generation.

The ratio between amplitude modulation and the resulting phase modulation may be quantitatively expressed by a coefficient $K_{am/pm}$. Taking C_{eff} as the mean value of the varactor, it is [14]:

$$K_{am/pm} = Q \cdot \frac{\partial C_{eff}}{\partial A_0} \cdot \frac{A_0}{C_{eff}} \qquad (6)$$

The conversion coefficient of the varactors can be assessed by simulations both behavioral and at transistor level (with Cadence SPICE). In the following we will comment only the latter results.

In the use SPICE one should remind that C_{eff}, is a quantity entering the expression:

$$\omega_0 = \frac{1}{\sqrt{L \cdot C_{eff}}} \qquad (7)$$

By changing I_P we vary A_0 and determine the period of oscillation; then, from Eq.(7) C_{eff} is easily extracted. Simulations have been performed at different biases of the tuning node; Fig. 9 shows the $K_{am/pm}$ dependence on A_0 when the varactors are reverse biased with 0.8 V.

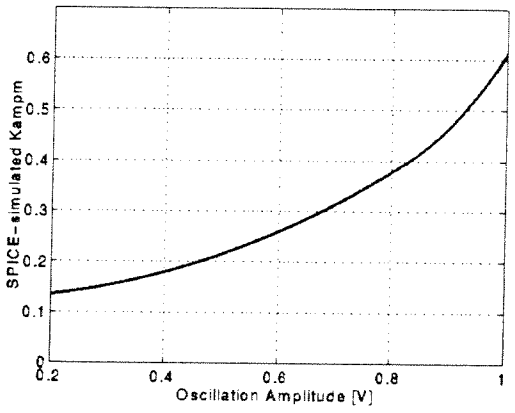

Fig. 9 - AM to PM conversion coefficient vs. oscillation amplitude

The contribution to the phase noise of the oscillator is obtained by multiplying the AM noise power reaching the tank for $K^2_{am/pm}$ and for the "shaping factor" $1/(2\alpha C)^2$ as already done in Eq.(1) for the thermal noise.

As an example, with the previous data, with a current I_P = 3.5 mA (i.e. oscillation amplitude A_0 = 0.5 V) and losses g_{ot}= 1/228 Ω^{-1} this AM-to-PM effect sets a SSCR at 3 MHz as high as -143 dBc/Hz, very close to the limit of the GSM standard. If we increase the amplitude A_0 to 1 V by increasing the bias current, the SSCR is even raised to the value of -136 dBc/Hz, threatening the feasibility of the overall design. Therefore there is a trade-off which maintains the AM-to-PM contribution below the required phase noise threshold, while satisfying the need for oscillation amplitude as high as possible.

Acknowledgments

The work has been supported by MURST (the Italian Ministry of University and Scientific and Technological Research) and by CNR (Italian National Research Council) in the framework of "Progetto Finalizzato MADESS II". We also wish to thank Francesco Villa for the work done during his degree thesis.

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