

# Development of a CMOS Cell Library for RF Wireless and Telecommunications Applications

Robert H. Caverly  
Department of Electrical and Computer Engineering  
Villanova University  
800 Lancaster Avenue  
Villanova, PA 19085

## Abstract

There is increasing interest in the use of CMOS circuits for highly integrated high frequency wireless telecommunications systems. This paper presents the results of on-going work into the development of a cell library that includes many of the circuit elements required for the high frequency sub-system of a communications integrated circuit. The cells were fabricated using standard MOSIS processes and measurement results are presented. The full design files, testing results and circuit tutorials describing the cells and how they interface with baseband circuits are available from the author.

## Introduction

At the heart of rapid integrated system design is the use of cell libraries for various system functions. In digital design, these standard cells are both at the logic primitive level (NAND and NOR gates, for example) as well as higher levels of circuit functionality (ALUs, memory). For baseband analog systems, standard cell libraries are less frequently used, but libraries of operational amplifiers and other such analog circuits are used. The use of analog CMOS circuits for use at high frequencies has garnered much attention in the last several years [1-11]. This paper will discuss the results of on-going work in the development of a library of CMOS cells using standard CMOS processes readily available to the microelectronic system's community.

In the design of a cell library, the cells must be designed to be flexible in terms of drive requirements and loading. For RF applications, the most common driving requirements for off-

chip loads are based on  $50\Omega$  source and load impedances. The systems designed and reported on here maintain this industry standard of  $50\Omega$  system compatibility. At the same time, since these cells are to be used with digital and baseband analog systems, they must be designed to be controlled by on-chip digital and analog signals. Consideration of these factors was used through the design of the library. The cells described in this paper can be used separately or combined to construct more complex functions such as an RF front end. Each of the cells will be discussed separately for the sake of clarity of presentation and understanding of the operation of the circuit.

The RF cell library presented here consists of cells designed, fabricated and tested using standard MOSIS 2.0, 1.2 and 0.8 micron CMOS processes. There was no post-processing performed on any of the circuit topologies presented in this paper. As additional assistance to the RF design community, the CIF layout files, test data and tutorials are available from the author.

## General Fabrication Comments

All the cells being investigated were fabricated using 2.0, 1.2 and 0.8 micron ( $\mu\text{m}$ ) silicon CMOS n-well processes using both n-channel and p-channel enhancement MOSFETs using MOSIS. The 2.0  $\mu\text{m}$  and 1.2  $\mu\text{m}$  silicon CMOS library elements were fabricated using the Orbit Semiconductor, Inc. process, and the 0.8  $\mu\text{m}$  elements were fabricated using a Hewlett-Packard process. Most of the designs utilized multiple gate fingers to help reduce parasitic capacitance in an effort to improve the frequency response.

## RF SPDT Switching Element

Single pole double throw (SPDT) switches have a variety of uses. A typical application of the SPDT switch would be the sharing of a single antenna between receiver and transmitter, with digital control voltages on the appropriate FET gates activating the appropriate switch branch. Figure 1 shows a schematic of the CMOS SPDT switch element, which is similar to other FET-based switching elements [12]. The SPDT switch was designed to exhibit low insertion loss in the on-state and high isolation in the off-state in a 50Ω system. The insertion loss of the switch element is directly related to the on-state resistance of the series switch element:

$$IL = 20 \log \left[ 1 + \frac{R_{ON}}{Z_0} \right] \text{ dB}, \quad (1)$$

Each gate finger of the switching element varied in width depending on the process used, from 4000 μm for the 2.0 μm process to 400 μm for the 0.8 μm process. Multiple gate finger widths were used in an effort to reduce parasitic drain and source sidewall capacitances. These parasitic capacitances are typically higher than their GaAs MESFET counterparts. The 0.8 micron SPDT switching element and input/output contacts (Figure 2) are approximately 432 by 322 microns. The 0.8 micron switching element without the contacts is approximately 100 by 85 microns. The larger gate length switch elements are physically larger since the smaller transconductance requires larger FETs to maintain low insertion loss in the switch on-state. The increased FET size, however, will negatively impact the off-state isolation because of the increased capacitance.

The on-state resistance of the CMOS switch elements is modeled using the following expression:

$$R_{ON} = \frac{L}{WK_P(V_{CTL} - V_T)} \quad (2)$$

where L is the gate length (2.0, 1.2 or 0.8 microns), W is the gate width,  $K_P$  is the intrinsic transconductance,  $V_{CTL}$  is the control voltage on the gate and  $V_T$  is the threshold voltage. The intrinsic transconductance  $K_P$  ranges from

approximately 50 μA/V<sup>2</sup> for 2.0 micron technologies to 125 μA/V<sup>2</sup> for the 0.8 micron devices. The threshold voltages for the devices were all in the 0.7 to 0.9 volt range. For a given value of on-state resistance, a combination of larger  $K_P$  and smaller gate length L allows smaller gate widths W to be used, thereby significantly reducing the overall size of the microwave and RF switching transistors and hence the entire switching element.

The 0.8 micron switch layout illustrated in Figure 2 is representative of the general layout of the SPDT CMOS switching elements. The RF common connection is along the top between the two ground connections. Along the bottom are the two input switch arms and the dc control ports.

## RF Performance

Switch measurements were performed on a combination of unpackaged and packaged experimental SPDT chips at frequencies to 2.0 GHz. Figure 3 shows the results of isolation and insertion loss measurements on the 0.8 micron SPDT CMOS switching elements. All three switch elements (2.0, 1.2 and 0.8 micron elements) exhibit low frequency insertion loss values less than 0.8 dB. Isolation for all the devices is greater than 50 dB at low frequencies, but degrades as frequency is increased. Much of the performance degradation at higher frequencies was caused by the package parasitics of the enclosure used. Performance data for the 0.8 μm device, the best technology of the three studied, shows 3 dB insertion loss and greater than 25 dB isolation at 1.0 GHz. The 1.2 micron element exhibited the 3 dB insertion loss point at approximately 500 MHz, while the 2.0 micron element exhibited 3 dB insertion loss at approximately 220 MHz. Measurements on the 1.2 and 0.8 micron control elements using a control voltage of 3.3 volts showed negligible differences in insertion loss and isolation over the frequency range. This lower control voltage makes these devices attractive for battery power applications. The next generation of switch elements to be fabricated will reduce the parasitic interconnect resistance to a level that will lower the insertion loss to approximately 0.5 dB.

Distortion performance was also measured for the CMOS SPDT switch element.

Measurements on the 1.2 micron element yielded distortion intercept point IP2 and IP3 values of approximately +39 dBm and +27 dBm, respectively, at 110 MHz. These values are comparable to intercept points for GaAs MESFET switches [13,14] and are expected to improve at higher frequencies.

### Series Reflective Attenuator Element

CMOS controllable RF signal attenuators were also tested using a series reflective configuration. Attenuation measurements were performed on the 2.0 and 1.2  $\mu\text{m}$  control elements by varying the gate control voltage ( $V_{CTL}$ ) over a 0 to 5 volt range. Figure 4 shows the results of these measurements at 100 MHz on the 1.2 micron element, indicating a useful attenuation range up to 10 dB. The data are plotted with an attenuation model for comparison. The 2.0 micron element exhibited similar behavior. The level of attenuation (ATT) is given by the following expression:

$$ATT = 20 \log \left[ 1 + \frac{R_{ON}}{2Z_0} \right] \text{ dB}, \quad (2)$$

where  $R_{ON}$  is the series resistance of the attenuator modeled using Equation 1 and  $Z_0$  is  $50\Omega$ . Note the minimal change in element characteristics over the 3 to 5 volt range, validating the use of these devices at lower control voltages.

### CMOS RF Amplifiers

Traditional RF and microwave amplifiers in use today are GaAs MESFET structures, or discrete silicon MOS and BJT devices. Any amplifier regardless of technology should have reasonable output power drive into a  $50\Omega$  load and low intermodulation distortion since in many applications, systems using these amplifiers in transmitter chains may be operating in close physical proximity to one another. Some work has been done on the use of silicon CMOS for highly integrated systems [1,6-11]. In much of this work, the MOS amplifying structures are either teamed with an integrated inductor that requires post-processing to improve the inductor

performance or with external chip inductors for bias isolation.

### Description of the Amplifier

Each RF amplifier (Figure 5) was designed to drive a  $50\Omega$  load. This low resistance load impedance requires physically large FETs since the intrinsic transconductance in CMOS FETs is significantly lower than either bipolar or GaAs technologies. Each FET in the amplifier utilized a number of separate gate fingers, the actual number depending on the geometry used. These gate fingers were chosen to help reduce the  $N^+$ -P area and sidewall capacitances of the source and drain diffusions in an effort to improve the frequency response. Each gate finger varied in length depending on the process used, with a total gate width of  $5000\mu\text{m}$  for the  $2.0\mu\text{m}$  process,  $3000\mu\text{m}$  for the  $1.2\mu\text{m}$  and  $2000\mu\text{m}$  for the  $0.8\mu\text{m}$  process. Measurements of insertion gain of these amplifiers indicated a low frequency gain of

$$IG = 2500 g_m^2 \quad (4)$$

for the  $50\Omega$  system.

### RF Performance

RF measurements on the  $2.0$  and  $1.2\mu\text{m}$  amplifiers were performed up to  $900\text{MHz}$  on the packaged devices. Measurements show that the output RF power of these devices is variable (depending on p-fet current source bias) up to  $+10.5\text{dBm}$  using a  $+5.0\text{V}$  power supply. Figure 6 shows the results of insertion gain measurements and simulations on the  $1.2\mu\text{m}$  RF amplifier. The current source bias (p-FET) and driver bias (n-FET) were varied to achieve the optimum gain. Also shown in Figure 6 are SPICE simulations of the amplifier's gain including test fixture parasitics as well as another set of simulations showing expected amplifier performance in a typical package more optimized for this amplifier. The  $2.0$  micron element showed similar low frequency insertion gain but a unity gain frequency of approximately  $500\text{MHz}$ .

Distortion measurements taken at  $135\text{MHz}$  on the  $1.2\mu\text{m}$  RF amplifier as a test of the

amplifier's linearity show second, third and fourth order intermodulation intercept points (referenced to the load) of 44 dBm, 23 dBm and 19 dBm, respectively. With a 10 dB input power, these distortion intercept points correspond to second, third and fourth order powers of -24 dBm, -16 dBm, and -17 dBm, respectively.

Measurements were also taken on a silicon CMOS SPDT-RF amplifier configuration feeding a 50  $\Omega$  load such as would be seen in an RF front-end application. The bias on the amplifier FETs was adjusted for maximum output power to the load. As expected, the insertion gain of the switch-amplifier combination was reduced by the insertion loss of the switch. The second and third order intercept points of the switch-amplifier combination were reduced from the values presented above by approximately 6 and 3 dB, respectively, primarily due to the distortion properties of the SPDT switch.

## CMOS RF Mixers

The RF mixer is used to either up-convert a baseband analog or digital signal for ease of transmission, or to down-convert a high frequency signal to baseband for ease of signal processing. The simplest mixer structure that combines good LO isolation with reasonable conversion gain in the singly balanced mixer (Figure 7). The LO cancellation occurs at the differential output of the mixer when the LO is fed in-phase at the input gates of the FETs, but the RF is fed 180 degrees out of phase. As opposed to conversion loss in passive diode mixers, well-designed transistor mixers can provide conversion. The 2.0 and 1.2 micron circuits, designed to drive 50 $\Omega$  loads, were tested for conversion gain up to 1000 MHz. At low frequencies, both technologies provided approximately 6 dB of conversion gain. At approximately 600 MHz, the 2.0 micron mixer exhibited 0 dB conversion gain, while the 1.2 micron mixer exhibited conversion gain up to approximately 950 MHz. These results indicate the 1.2 micron elements suitable for applications up to cellular telephone frequencies. As a final note, other mixer circuit topologies are possible using CMOS technology [1,2].

## Conclusions

This paper presented the results of on-going work done in preparing a library of 2.0, 1.2 and 0.8 micron CMOS cells for use at frequencies above 500 MHz. Figure 8 shows the layout of the integrated circuit containing the 0.8 micron circuit structures. The results indicate that 1.2 micron library cells have a useful range that includes the cellular telephone band around 900 MHz. Higher frequency ranges are indicated using the 0.8 micron cells, including the important commercial band pertaining to global positioning systems. Lower frequency operation at IF frequencies are possible using the 2.0 micron circuits. These cells are available from the author along with full test results. Further work is underway in improving the performance this CMOS cell library. These performance enhancements include improving the insertion loss and isolation properties of the CMOS 50 $\Omega$  switch element, improving the frequency response of the RF amplifiers and the testing of an already fabricated Gilbert cell mixer in the three technologies.

## Acknowledgment

This material is based upon work supported by the National Science Foundation under Grant No. MIP-9414308. Additional assistance in measurement goes to G. Hiller of Alpha Industries, Woburn, MA and Scott Smith of the ECE Department at the University of Massachusetts Dartmouth.

## References

1. N. Camilleri et al., "Silicon MOSFETs, the microwave device technology for the 90s", 1993 *IEEE Intl. Microwave Symp. Digest*, p. 545, 1993.
2. B-S. Song, "CMOS RF Circuits for Data Communications", *J. Solid-State Cir.*, vol. SC-21(2), pp. 310-317, 1986.
3. Manetakis, K.; Park, S.-M.; Payne, A.; Setty, S.; Thanachayanont, A.; Toumazou, C., Wideband CMOS analog cells for video and wireband communications, *IEE Colloquium on Wideband Circuits, Modelling and Techniques* May 10 1996 n 111, p 6/1-6/10

4. Robert H. Caverly G. Hiller, A Silicon CMOS Monolithic RF and Microwave Switching Element, *Proc. 1997 European Microwave Conference*, Sept., 1997.
5. P. R. Gray, *Future Directions in Silicon ICs for RF Personal Communications*, CICC, 1995.
6. Abidi, A. CMOS-only RF and Baseband Circuits for a Monolithic 900 MHz Wireless Transceiver, *Proceedings of the IEEE Bipolar/BiCMOS Circuits and Technology*, p 35-42 1996.
7. Kokozinski, R. ; Barthel, W. ; Brockherde, Werner ; B., Wolfram ; H., Bedrich J. ; Zimmer, G. , Microwave Wideband Amplifiers in Bulk-CMOS and CMOS/SiMOX, *Proceedings of the 1995 IEEE International Solid-State Circuits Conference* Feb 15-17 1995 v 38 Febr p 188-189
8. J. Y-C. Chang and A. A. Abidi, A 750 MHz RF Amplifier in 2- $\mu$ m CMOS, *Symposium on VLSI Circuits Digest of Technical Papers*, 1993
9. Rofougaran, A. ; Chang, J. Y.-C. ; Rofougaran, M. ; Abidi, A., 1 GHz CMOS RF Front-end IC for a Direct Conversion Wireless Transceiver, *Proceedings of the 1995 21st European Solid-State Circuits Conference*, Sep 19-22 1995 v 31 n 7 p 880-889
10. Rofougaran, M. ; Rofougaran, A. ; Olgaard, C. ; Abidi, A.A. , 900 MHz CMOS RF Power Amplifier with Programmable Output, *Proceedings of the 1994 Symposium on VLSI Circuits* Jun 9-11 1994 p 133-134
11. J. Y-C. Chang, A. A. Abidi, and M. Gaitan, Large Suspended Inductors on Silicon and their use in a 2- $\mu$ m CMOS RF Amplifier, *IEEE Electron Device Letters*, v. 14, 1993
12. Ayalsi, Y., "Microwave Switching with GaAs FETs", *Microwave J.*, vol. 25, pp.61-71, Nov. 1982.
13. R. H. Caverly , "Distortion in GaAs MESFET Switches", *Microwave Journal*, pp. 106-114, Sept., 1994.
14. R. H. Caverly , "Distortion in Broadband Gallium Arsenide MESFET Control and Switch Circuits," *IEEE Trans. Microwave Theory and Techniques*, vol. 39(4), pp. 713-717, April, 1991.

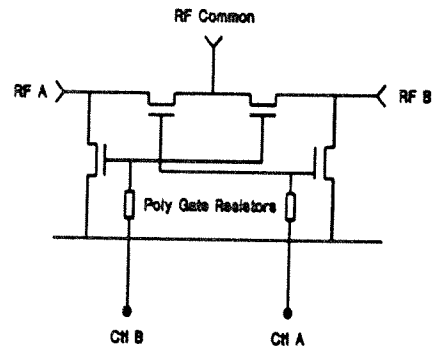


Figure 1. Schematic diagram of the SPDT microwave and RF switching element. The same circuit topology is used for all technologies; only the physical size of the FETs are different.

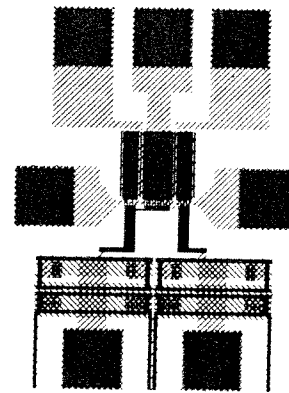


Figure 2. Mask level layout of the 0.8 micron SPDT CMOS microwave and RF switch with input/output contacts shown.

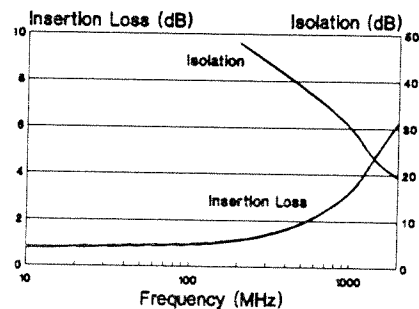


Figure 3. Insertion loss for the 0.8 micron SPDT CMOS switch. Isolation was greater than 20 dB all frequencies below 2000 MHz.

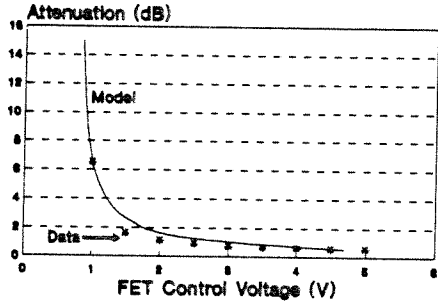


Figure 4. Attenuation characteristics of the 1.2 micron switching element in an attenuator configuration versus gate control voltage.

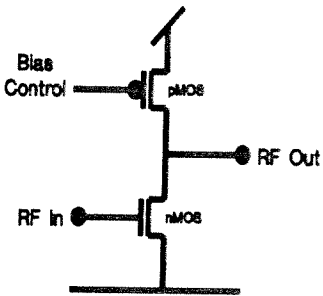


Figure 5: CMOS 50Ω RF amplifier. The same circuit topology was used for all three technologies studied.

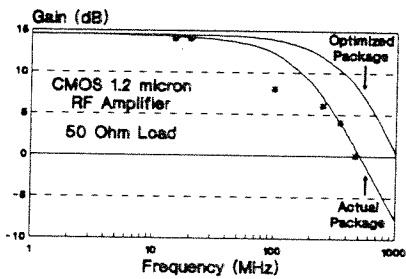


Figure 6. Frequency Response of the 1.2 μm integrated CMOS RF amplifier.

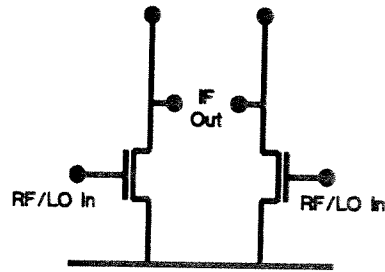


Figure 7. Schematic diagram of a general singly balanced CMOS mixer. Conversion gain was measured up to approximately 950 MHz for the 1.2 micron element and 600 MHz for the 2.0 micron element.

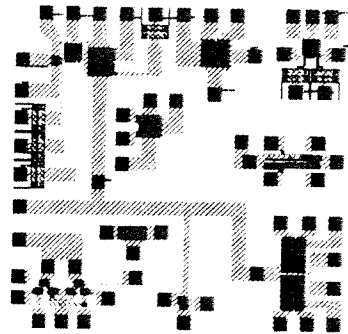


Figure 8. Full die view of the 0.8 micron CMOS RF cell library integrated circuit.