A Bootstrapped NMOS Charge Recovery Logic

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Abstract

This paper describes a new Bootstrapped NMOS Charge Recovery Logic (BNCRL) which realizes low energy computation. Power comparison with a state-of-the-art adiabatic charge recovery circuit is shown for an inverter chain and an 8-bit adder. The new logic circuits exhibit full rail-to-rail logic swing, less dependency of energy consumption on output load capacitance variations, and significant energy saving. Benchmark circuits were designed for comparison using 0.6-μm CMOS technology.

1 Introduction

Power consumption in electronic devices has become an important issue as the density of integrated circuits increases rapidly. Low power consumption is considered most crucial in consumer electronics, in particular portable computers and wireless phones since the battery life time prevails in such products. Thus, the circuit design based on adiabatic techniques and charge recovery is attractive because of drastic reduction in energy consumption. In such circuits, low energy consumption is realized by operating circuits with small potential differences across the channels of transistors during computation and by using an ac power supply instead of dc for charge recovery.

Several adiabatic charge recovery circuits have been proposed and their potential for practical applications has been demonstrated [?] – [?]. Previous circuits have used diodes and diodes-like devices or PMOS transistors for delivering or recovering charge. In those circuits, energy loss is due to voltage drops across the diodes while precharging output nodes and incomplete charge recovery through PMOS transistors from an output node. Thus a small diode turn-on voltage or a small MOS threshold voltage is required to achieve low energy consumption. Also, their energy dissipation is proportional to output load capacitance.

We have developed new adiabatic charge recovery circuits with bootstrapped NMOS transistors. These circuits exhibit full rail-to-rail logic swing, less dependency of energy consumption on output load capacitance, and significant energy saving over other adiabatic charge recovery circuits.

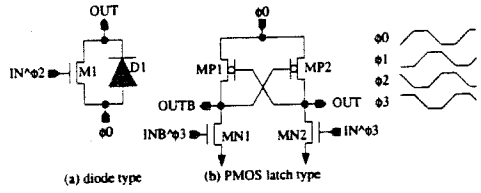

Figure 1: Previous adiabatic inverter circuit

This paper is organized as following. In Section 2, circuit concept and basic operation are discussed. In Section 3, energy comparison and simulation results for an inverter chain and a pipelined 8-bit adder are shown. Finally, Section 4 presents our conclusion.

2 Circuit Concept and Basic Operation

Two types of previous adiabatic charge recovery circuits are shown in Fig.1. In a diode-type, diode or a diode-like device(D1) is used for precharging an output node at the rising phase of $\phi 0$ and logic is evaluated and charge is recovered through the NMOS transistor(M1) at the falling phase of $\phi 0$ according to an input signal(IN$\wedge\phi 2$) which has the same clock phase as $\phi 2$. Since output precharge is done through the diode, high logic level is degraded to $V_{dd} - V_{d,on}$, where $V_{d,on}$ is the diode turn-on voltage. In a PMOS_latch_type, during the rising phase of $\phi 3$, one of inputs(IN$\wedge\phi 3$ or INB$\wedge\phi 3$) which has the same clock phase as $\phi 3$ makes one of the PMOS drivers turned on. Clock $\phi 0$ is used to evaluate logic and recover the delivered charge. Since PMOS transistors are used for recovering charge, the stored charge can not be recovered fully.

The bootstrapped NMOS charge recovery logic (BNCRL) that we propose is shown in Fig. 2. It has circuit structure with complementary outputs (OUT & OUTB) since the matching of effective capacitive loading on each ac power clock during various logic operation is desirable for charge recovery logic with ac power clocks. The proposed circuit is composed of bootstrapped NMOS transistors (M1 & M6) with separate control paths (M2,M3 & M7,M8 for precharge and isolation and M4,M5 & M9,M10 for discharge). Three clock signals each with a 90° phase difference are used for each logic computa-

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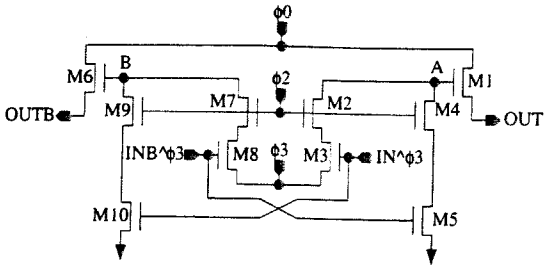

Figure 2: Proposed bootstrapped NMOS charge recovery logic(BNCRL) - an inverter

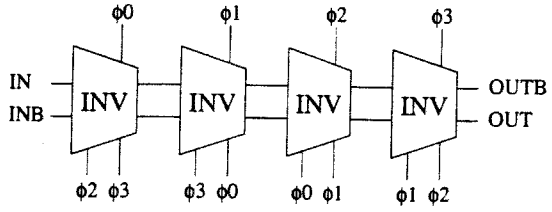

Figure 3: Clock distribution to BNCRL.

tion. Two ($\phi 2$ & $\phi 3$) are for precharging a bootstrapping node (A or B) and keeping its voltage level high enough to transfer charge completely and recover used charge. The other ($\phi 0$) is for transferring charge to the output node. Next three clock signals follow with a 90° phase lag respectively. A set of 4 power clocks each with a 90° phase difference are required for a complete full pipelined operation. The clocking rule applied to an inverter chain is shown in Fig. 3.

Fig. 4 illustrates the corresponding detailed timing diagram and simulated node waveforms. Trapezoidal clock waveforms are chosen for convenience. But in reality they can be sinusoidal. Before starting logic computation, all output nodes are set to ground. Clock $\phi 2$ turns on isolation transistors (M2, M4, M7 & M9) during t1 before input signals arrive.

Other transistors (M3&M10, M5&M8) are turned on during t2 according to input signals. Inputs may come from external circuits or previous stages in the pipelined architecture, which have the same phase as $\phi 3$. For example, let us assume that input signals come from the previous stage, IN is high and INB is low. According to input signals, node A is precharged to $V_{dd} - V_{tn}$ and node B is set to low. When the previous logic state is different from the present one, node B precharged at $V_{dd} - V_{tn}$ is discharged to ground through M9 & M10. This gate charge which is discharged for the different logic computation is the major portion of the energy dissipation in BNCRL.

When the valid source clock $\phi 0$ arrives, the gate of the clock-pass transistor(M1) is bootstrapped to a voltage higher than V_{dd} and logic high level is transferred to the node OUT in full strength. This output signal is maintained for a while and used as an input for the next stage. During t3, clock $\phi 2$ goes down and M2, M4, M7 & M9 turn off. Since clock $\phi 2$ isolates the bootstrapping node from other nodes, the bootstrapping efficiency is not degraded and the charge at the gate of M1 can also be kept for charge recovery. Without the isolation function

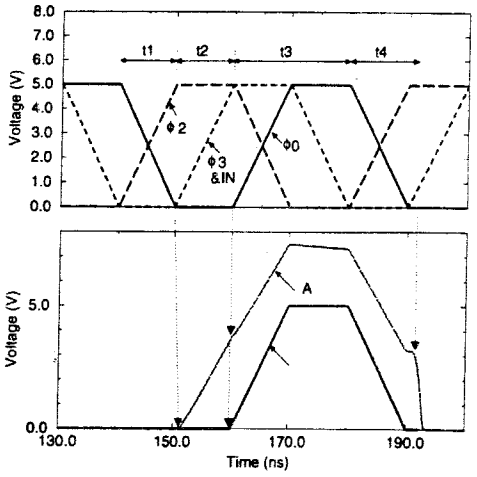

Figure 4: Timing diagram and simulated node waveforms.

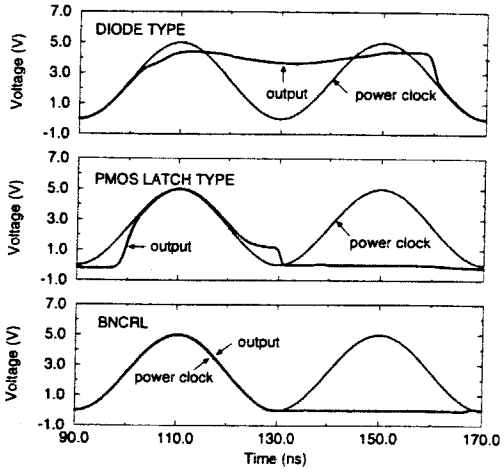

Figure 5: Output waveforms for sinusoidal power signal clocks.

of M2, the bootstrapping efficiency would be lowered due to larger junction capacitance when logic functions such as AND shown in Fig.9 are implemented. This would require larger bootstrapping transistors and increases energy consumption.

During t4, delivered charge is recovered in the adiabatic manner when $\phi 0$ goes down. Since charge at the node A is kept intact, transferred charge except the charge of the bootstrapped gate in the next stage can be fully recovered through M1.

The ac power clock signals typically have sinusoidal waveforms. The output waveforms of the inverter chain of various adiabatic circuits are shown in Fig. 5. As mentioned earlier, BNCRL shows full rail-to-rail logic swing, better adiabatic charge transfer and recovery than other adiabatic charge recovery circuits.

BNCRL has bootstrapping NMOS transistors which have separate control paths for precharging and discharging. Full rail-to-rail logic swing with completely adiabatic charge delivery and full charge recovery except the charge in the bootstrapped gate are realized by controlling the isolation transistors. Through control, the bootstrapping operation is kept effi-

cient for charge delivery and the bootstrapping node is retained for charge recovery.

3 Performance Comparisons

3.1 Energy Comparison for an Inverter Chain

The energy loss of conventional CMOS logic is

$$E_{CMOS} = C_{load}V_{dd}^2 + E_{short} \quad (1)$$

where C_{load} is the load capacitance, and E_{short} is energy loss due to short circuit current during transition. Even though energy dissipation in previous adiabatic circuits is much smaller than that of CMOS logic, energy loss due to diode precharging for output nodes and incomplete charge recovery through PMOS transistor are inevitable. Their energy losses are

$$E_{DIODE\_TYPE} \simeq C_{load}V_{dd}V_{d,on} + E_{opd} \quad (2)$$

$$E_{PMOS\_LATCH\_TYPE} \simeq \frac{1}{2}C_{load}|V_{tp}|^2 + E_{opp} \quad (3)$$

where $V_{d,on}$ is the diode turn-on voltage, V_{tp} is the PMOS threshold voltage, E_{opd} and E_{opp} are energy consumptions during logic computation in diode precharge type and PMOS_latch_type adiabatic charge recovery circuits, respectively. Since the energy consumption of BNCRL is due to diode-like precharging for a bootstrapping gate and the gate charge which is discharged to ground during t4 for different logic computation, its energy loss can be expressed as

$$E_{BNCRL} \simeq \frac{1}{2}C_gV_{tn}(V_{tn} + V_{dd}) + E_{ofb} \quad (4)$$

where C_g is the gate capacitance of the bootstrapping transistor, V_{tn} is the threshold voltage of the isolation transistor, and E_{ofb} is energy loss due to nonadiabatic precharging of the bootstrapping node. But because the capacitance of the bootstrapping node is much smaller than that of the output capacitance, energy loss is reduced drastically.

Fig.6 illustrates the energy dissipation of BNCRL inverter chain compared with that of the PMOS_latch_type since both of them can provide full rail-to-rail logic swing. Optimized transistor sizes are used in each logic circuit for comparison. Four trapezoidal supply clocks with a 90° phase difference and equal time for each phase are used. Output load consists of signal line capacitance and transistor gate capacitance. Since BNCRL transfers adiabatically and recovers all charge fully except the gate charge of the bootstrapping transistor, energy dissipation is reduced greatly and it is far less dependent on output load capacitance. BNCRL is more effective for larger load capacitance.

A drawback of BNCRL is the limit of operating voltage for the bootstrapping operation. In the low voltage, the bootstrapping efficiency is degraded due to the lowered precharge level at the gate of the bootstrapped transistor and thus energy consumption increases. Energy dissipation for various operating voltages of an inverter chain is shown in Fig.7. Since the 5V-technology transistors are used for comparison purpose BNCRL shows the increase of energy consumption below 3.5V, and full logic level is not delivered to the output node below 3V. But its energy saving is still large.

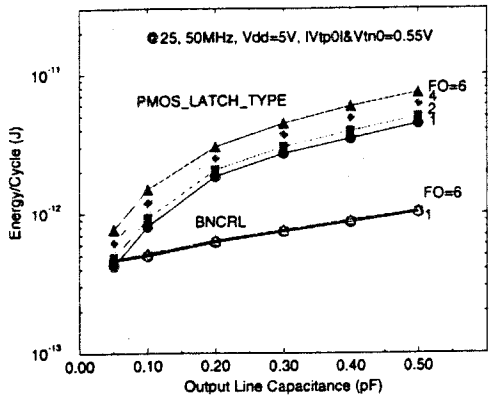

Figure 6: Power consumption comparision for load capacitance.

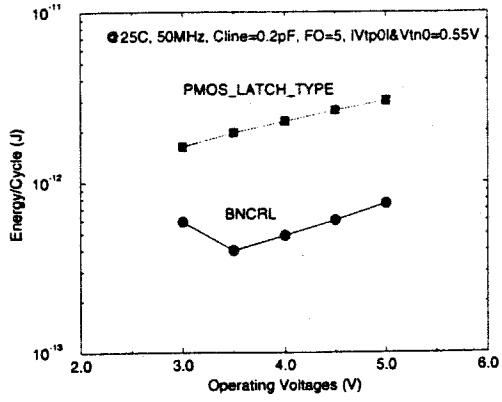

Figure 7: Power consumption comparision for operating voltages.

3.2 Energy Comparison for an Adder

For practical applications, it is required that for the proposed circuit design method be amenable to implement various logic functions. Various logic can be constructed similar to CMOS logic except that each PMOS transistor is replaced by an NMOS transistor with complementary input signals and a bootstrapping driver which has isolation transistor controlled by another ac clock $\phi 2$. Complementary logic structure is required for the complementary output. The implementation of 2-input AND logic according to this rule is shown in Fig. 8.

An 8-bit adder with a pipelined architecture has been implemented using the PMOS_latch_type and BNCRL circuits. The number of transistors to implement the 8-bit adder is 492 for the PMOS_latch_type and 1006 for BNCRL. While the number of transistors increases by two times to implement the adder with BNCRL logic, the layout area penalty is not significant. This is due to the fact that only NMOS transistors are used and small sizes of transistors are used for controlling the gate of bootstrapping transistors. Energy dissipation for adder is shown as a function of operation frequencies in Fig. 9. Energy saving is significant over a wide range of operating frequency from 25 to 100MHz. It is approximately 50% at 100MHz op-

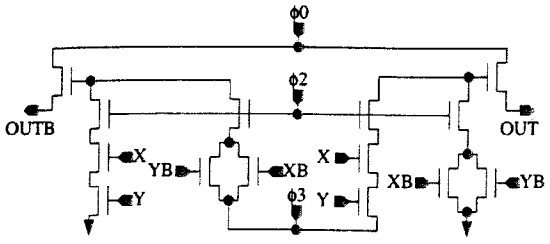

Figure 8: Logic implementation for *AND* gate.

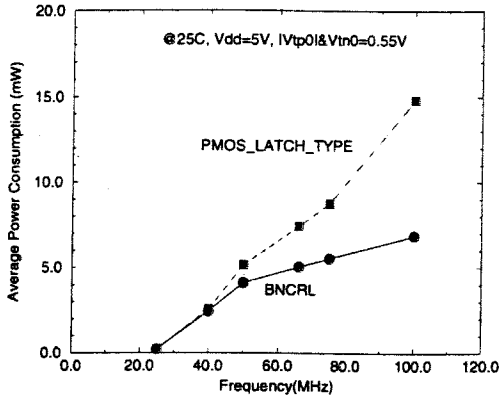

Figure 9: Energy comparison for an 8-bit adder.

erating frequency. Fig. 10 illustrates the layout of the fully functional 8-bit adder implemented by BNCRL.

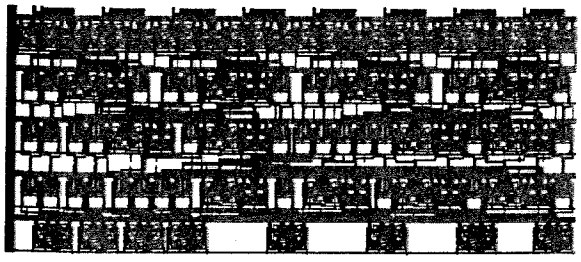

Figure 10: Layout of a BNCRL 8-bit adder.

4 Conclusions

We proposed a new Bootstrapped NMOS Charge Recovery Logic(BNCRL) composed of bootstrapped NMOS transistors whose gates have separate precharge and discharge paths and isolation transistors which are controlled by ac clocks for efficient bootstrapping and charge recovery. BNCRL shows full rail-to-rail logic swing, and more effective charge transfer and charge recovery, resulting in low energy computation. BNCRL also shows less dependency of energy consumption on output load capacitance variations. An inverter chain and an 8-bit adder have been implemented and significant energy saving is proven by simulation.

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