Organizer: Jonathan Rose, University of Toronto.
Moderator: Sinan Kaptanoglu, Actel Corporation
Panelists:
  Jonathan Rose, University of Toronto (the academic)
  Clive McCarthy, Altera Corporation (the architect)
  Rob Smith, Actel Corporation (the software developer)
  Sandip Vij, Xilinx Corporation (the marketing representative)
  Steve Taylor, Nortel Corporation (the customer)

Panel Discussion:

The FPGA development is an extraordinarily complex task, involving many people working in architecture, chip design, software, marketing and production. Each tends to focus on their immediate task, and have their own measures of goodness for what they do, as well as very particular constraints relevant to their discipline. In this panel we will discuss these measures and constraints in an attempt to see how they succeed in transcending the artificial borders in each discipline.

An FPGA customer presents a set of impossible demands: create a chip that will do whatever he wants, and do it as cheaply as possible, run at the required speed, be available in the right package and have an easy to use software that does everything automatically with no manual intervention and no design iteration.

An FPGA architect tries to meet some of these demands. He must address the needs of the greatest number of customers, many of which may be conflicting. What are his metrics? Early on in the architecture development, when tools may not be available, how does he make decisions? What are the constraints that force particular types of decisions? What about later?

Although software development and architecture go hand in hand, the software group brings additional constraints to the table: having to maintain large chunks of code in the face of major new architectures, interface and integration of external tools supplied by CAD vendors (schematic capture, synthesis, simulation, etc.) What measures of goodness are applied in the software development and integration process? How do these affect architectural decisions?

Marketing often plays the role of representing the customer, by relaying his demands to the architects and other developers. What is marketing’s true goal? Depending on whether Dilbert holds sway or not, this can be a nefarious or an inspired role.

Academics seeking to add knowledge to the community often create various metrics to measure the goodness of their own work such as track count, pin count, logic block count, area models, net delay, path delay, published paper count, happiness of funding agency representatives, etc. Do any of these reflect reality that will convey true knowledge?

Operations also have their concerns with regard to yields, wafer sort, testing, packaging, and even inventory and shipping. How do these concerns define a measure of goodness for FPGAs?

Finally, there is the long-term health of the FPGA industry itself. Have we made progress against gate arrays and standard cells? Will the micro-processor sneak up and bite us from behind?