Characterization-Free Behavioral Power Modeling

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Abstract
We propose a new approach to RT-level power modeling for combinational macros, that does not require simulation-based characterization. A pattern-dependent power model for a macro is analytically constructed using only structural information about its gate-level implementation. The approach has three main advantages over traditional techniques: i) it provides models whose accuracy does not depend on input statistics, ii) it offers a wide range of tradeoff between accuracy and complexity, and iii) it enables the construction of pattern-dependent conservative upper bounds.

1 Introduction
Modeling power consumption at high level of abstraction is a challenging issue that has received considerable attention in the last few years. Several efforts have focused on the development of power models for combinational macros which are the functional building blocks of complex designs described at the register-transfer level (RTL). As a result, several power models have been proposed ranging from constant estimators of the average power consumption [1] to advanced models that try to capture the dependence of power dissipation on the input patterns applied to the circuit [2, 3].

The dependence on input pattern distribution is a well-known property of power consumption in CMOS circuits. Advanced power models take this effect into account. We can distinguish two classes of approaches. Pattern-independent models provide average power estimates based on a compact description of the input statistics, i.e., input transition activities and static probabilities [4, 5]. In contrast, pattern-dependent models provide a pattern-by-pattern power estimate during simulation [2, 3]. Pattern-dependent models are potentially more accurate than pattern-independent ones, and they can be used to estimate peak power as well as average power dissipation. On the other hand, they are more complex and may require long simulation runs to provide significant estimates.

Both pattern-dependent and pattern-independent models require characterization. Characterization consists of tuning model parameters in order to fit a sample of power consumption data provided by a gate-level (or switch-level) simulation of the implementation of the macro. If the RTL design is based on a given library of functional macros, characterization is performed once for all for each macro in the library and the resulting model is used to backannotate its functional description. During design exploration and RTL simulation, the same model is used to provide power estimates for all instances of the same macro.

Simulation-based model tuning (i.e., characterization) is attractive and practical: in principle it automatically increases the accuracy of power models to match that of a low-level simulator. Unfortunately characterization has two drawbacks that come from its statistical nature: i) it cannot guarantee out-of-sample accuracy, and ii) it does not enable worst-case evaluation.

1.1 Out-of-sample accuracy
We call out-of-sample accuracy the accuracy of a model evaluated for input conditions statistically different from those in which it was characterized. In contrast, we call in-sample accuracy the accuracy of a model evaluated in the same conditions used for characterization. Only in-sample accuracy is increased by the characterization process. If the input patterns applied to the circuit during characterization are not representative of the actual operating conditions, the model may produce unpredictable errors.

To improve out-of-sample accuracy two approaches have been attempted: increase the complexity (and the flexibility) of the model [4, 6, 2], or improve the characterization procedure [5, 7]. No general solutions have been provided by the first approach: when the model complexity increases the characterization process becomes even more critical and the resulting model prone to out-of-sample errors.

The second approach has been more successful [5, 7]. In [5] the authors proposed the usage of a look-up table (LUT) of constant estimators statically pre-characterized under different input-output conditions.

The method presented in [7] relies on the availability of a multilevel simulation environment to perform dynamic model tuning by means of an adaptive algorithm (namely, the LMS). Adaptive modeling achieves sizable improvements over the accuracy of statically-characterized equivalent models.

1.2 Worst-case evaluation
Even if it is possible to successfully trade off model complexity and/or characterization effort for out-of-sample accuracy, no compromises are allowed when dealing with worst-case estimates. Simulation-based characterization does not provide conservative worst-case estimators, unless an exhaustive search is performed by simulating all possible input transitions, i.e., all possible pairs of input patterns. Needless to say, this is unfeasible even for small circuits.

To perform conservative worst-case estimates, analytical approaches are required that look at the inner structure of a macro in order to find the input conditions that maximize its internal switching activity [8, 9]. Unfortunately,
the complexity of the problem grows exponentially with the number of inputs and gates in the circuit, and the exact solution can be found only for small circuits. For large combinational blocks, only conservative approximations are provided.

Independently of the accuracy of worst-case power estimates achievable for the macros, large errors are always introduced when estimating the worst case consumption of an entire RTL design which contains many instances of library macros. In fact, the knowledge of worst-case power consumptions of library elements provides little practical information about the power consumption of the entire design. No compensation occurs when adding conservative estimates, the overall error grows with the number of system components.

Pattern-dependent upper bounds can provide more significant (still conservative) worst-case power estimates at the RT level. Given an input pattern, it is possible to compute an upper bound to the power consumption of the entire circuit for that pattern by simply summing the pattern-dependent upper bounds of its components. Such bound is much tighter than what could be obtained by just summing the overall worst-case power consumption of all macros in the circuit. In this paper we present an analytical approach to pattern-dependent power modeling that:

- provides power models whose accuracy does not depend on the input statistics,
- provides pattern-dependent upper-bounds,
- effectively trades off accuracy for complexity.

In sharp contrast with all previous approaches our modeling procedure exploits information on the internal structure of the combinational logic unit. While in the past only black box models have been investigated, we propose a white box methodology. The modeling task is addressed in the next section. We discuss the modeling assumptions, we describe the RTL model and we outline a symbolic algorithm for its automatic construction. Approximation criteria and algorithms are discussed in Section 3. Experimental results are reported in Section 4. Section 5 concludes the work.

2 RTL power modeling

Fig. 1 shows a combinational unit (U) with inputs \( \mathbf{x} = [x_1, ..., x_n]^T \). We assume that the unit is stable at time \( t^i \) and \( t^f \) (\( t^f > t^i \)) and that an input transition from \( x^i \) to \( x^f \) occurs between \( t^i \) and \( t^f \). We denote by \( e(x^i, x^f) \) the supply energy drawn by the circuit in the time interval \([t^i, t^f]\). The task of modeling power consumption at the RT level consists of finding a simple but accurate model for \( e(x^i, x^f) \) (the corresponding power consumption being \( p(x^i, x^f, T) = e(x^i, x^f)/T \), where \( T = t^f - t^i \)).

In previous approaches, models are constructed by: i) observing input-output information, ii) performing highly accurate simulation to estimate the power dissipation that corresponds to a given input transition, iii) correlating the power measurement and the input-output transition pattern with some model-fitting procedure. Our approach is radically different. We do not perform simulation, but we directly construct a high-level model starting from a low-level description of the internal structure of the combinational unit, which we call golden model. It is important to notice that the golden model must be available for the characterization-based approaches as well, because it is required for performing accurate simulations.

There are many phenomena that contribute to \( e(x^i, x^f) \). For convenience, we partition them into structural and parasitic phenomena. For a given golden model of the unit, we call structural (parasitic) phenomena those phenomena that can (cannot) be appreciated at the abstraction level at which the golden model is provided. Power modeling and characterization are abstraction processes. The abstract model they provide cannot be more accurate than the golden model itself. Hence, the only phenomena that can be modeled are those that are structural for the golden model.

Characterization-based models are flexible because they can leverage any low-level simulator. In other words, they can be applied to any golden model (i.e., a gate-level netlist, a transistor-level description). We give up some flexibility. We assume that our golden model is a gate-level netlist with backannotated capacitances and zero propagation delays. At this level, the only structural phenomena are the supply currents that charge capacitances associated with raising signals. Their contribution to the overall energy is usually called dynamic consumption. Short-circuit currents, internal charge redistributions and spurious transitions (glitches) are all parasitic phenomena.

By choosing an abstract golden model, we loose some absolute accuracy. Two observations motivate this choice. First, absolute accuracy is not always a key feature at the RT level. During RTL design some absolute accuracy may be lost if relative accuracy is still satisfactory. Second, if absolute accuracy is required, characterization can be used in conjunction with our approach to capture parasitic phenomena.

Our modeling approach is not in contrast with characterization methodologies. On the contrary, it lends to a useful partitioning of the modeling task. We construct a model for the pattern dependency of zero-delay dynamic power, which is the structural power of our golden model. Dynamic power (that usually represents the largest contribution) is responsible for most of the pattern dependence of the overall power consumption. Parasitic phenomena have a similar (and usually smoother) dependence on input statistics. Once a robust RTL model has been analytically constructed for the structural power, characterizing parasitic phenomena is much simpler than characterizing...
the entire power consumption as a whole.

2.1 Analytical model construction

The structural power consumption of a zero-delay gate-level netlist can be expressed as

$$ \epsilon(x^{'}, x^{f}) = V_{dd}^2 C(x^{'}, x^{f}) $$

where $C(x^{'}, x^{f})$ represents the total switching capacitance (i.e., the total capacitance associated with signals that have a raising transition in the time interval $[t^{'}, t^f]$) and $V_{dd}$ is the supply voltage. Since we assume $V_{dd}$ to be constant, our modeling task consists of finding a RTL model for $C(x^{'}, x^{f})$. Fig. 1 shows a generic internal gate $g_i$ and its load capacitance $C_j$. If we denote by $S_N$ the set of gates having an output raising transition between $t'$ and $t_f$, the total switching capacitance is

$$ C(x^{'}, x^{f}) = \sum_{g_j \in S_N} C_j $$

Pattern dependence is implicit in the definition of $S_N$:

$$ S_N = \{g_j, j \leq N | g_j(x^{'}) = 0 AND g_j(x^{f}) = 1\} $$

where $g_j(x)$ is the output function of gate $g_j$ and $N$ is the total number of gates in the circuit. Since $g_j$ belongs to $S_N$ if and only if $g_j(x^{'})g_j(x^{f}) = 1$, we can re-write $C$ as:

$$ C(x^{'}, x^{f}) = \sum_{j=1}^{N} g_j(x^{'})g_j(x^{f})C_j $$

Example 1 Consider the simple netlist of Fig. 2.a. Its node functions are: $g_1(x) = x^{'}, g_2(x) = x_2$ and $g_3(x) = x_2 + x_1$. Assume that $C_1 = 40 fF, C_2 = 50 fF$ and $C_3 = 10 fF$. The total switching capacitance corresponding to an input transition from $x^{'} = 11$ to $x^{f} = 00$ is given by:

$$ C(11, 00) = g_1(11)g_2(00) \cdot 40 fF + g_2(11)g_3(00) \cdot 50 fF + g_3(11)g_3(00) \cdot 10 fF $$

$$ = 1 \cdot 1 \cdot 40 fF + 1 \cdot 1 \cdot 50 fF + 0 \cdot 0 \cdot 10 fF $$

$$ = 90 fF $$

Example 2 Consider again the gate-level netlist of Fig. 2.a. Its node functions are: $g_1(x) = x^{'}, g_2(x) = x_2$ and $g_3(x) = x_2 + x_1$. Assume that $C_1 = 40 fF, C_2 = 50 fF$ and $C_3 = 10 fF$. The total switching capacitance corresponding to a given input transition (e.g., from $x^{'} = 11$ to $x^{f} = 00$) can be read directly from the corresponding row of the table ($C = C_1 + C_2 = 90 fF$).

In principle, Eq. (4) is the RTL model of $C$ we are looking for: as long as the logic functions realized at each internal node are known, it represents the switching capacitance as a function of $x^'$ and $x^f$. In practice, however, Eq. (4) is too complex to be used at the RT level. Its representation is much larger than the gate-level netlist we want to abstract away (N arbitrary Boolean functions of n variables, instead of N elementary gates), and its evaluation is more complex than a gate-level simulation ($\approx N$ instead of $N$). Moreover, Eq. (4) actually represents the implementation of the unit. If the unit is a third-party intellectual property (IP), Eq. (4) cannot be used to backannotate the functional description, or otherwise the IP would be violated. To obtain a RTL power model of practical interest we need to precompute the weighted sum at the right-hand side of Eq. (4), thus obtaining a direct representation of $C(x^{'}, x^{f})$.

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$C(x^{'}, x^{f})$ is a discrete function, i.e., a mapping from a Boolean space to a finite set of values, $V$ (notice that Boolean functions are nothing but discrete functions with $V = \{0, 1\}$). Boolean functions can be represented as binary decision diagrams (BDDs) [10], generic discrete functions can be represented as algebraic decision diagrams (ADDs) [11]. Fig. 3 shows the BDDs of the node functions of unit $U$ of Fig. 2.a and the ADD of its switching.
capacitance. The root of a decision diagram is the function it represents. Internal nodes are associated with input variables, edges represent input assignments, leaves represent output values. Any configuration of input variables corresponds to a path from the root to a leaf. Bold lines are used in Fig. 3.b to point out the path associated with $x^i = 13$, $x_f = 00$. According to Eq. 1, the corresponding leaf has value $90$.

Decision diagrams are ordered (variables are always encountered in the same order along any path) and reduced (isomorphic subtrees can be shared). Variable ordering makes the representation canonical, reduction makes it compact. Reduced, ordered decision diagrams provide an efficient way of representing and manipulating discrete functions. Logic and arithmetic operators are defined on BDDs and ADDs, respectively. From an algorithmic point of view, they take advantage of the structured representation to perform logic and arithmetic operations without actually enumerating all input configurations (i.e., symbolically). The number of elementary operations involved is linear or quadratic in the number of nodes in the diagram, rather than exponential in the number of variables. Though the worst-case complexity of the representation of a discrete function is inherently exponential, reduced ADDs usually provide much more efficient representations.

We don’t describe ADDs and BDDs in further details (the reader can refer to [11], [10]), but we rely on their properties for the symbolic manipulation and representation of discrete functions. Symbolic manipulation enables the straightforward implementation of Eq. (4): the ADD of $C(x^i, x_f)$ can be directly obtained by applying Eq. (4) to the BDDs of the unit’s node functions. Once constructed, the ADD can be evaluated in linear time for given input assignments.

To summarize, ADD-based symbolic modeling provides effective solutions to three of our modeling issues: i) it hides the dependence of $C$ on the internal functions, ii) it avoids exhaustive precomputation and iii) it enables runtime model evaluation in a negligible time (linear in the number of input variables).

A last issue needs to be addressed: the model complexity. Unfortunately, this is not a marginal problem. Decision diagrams may blow up exponentially when the number of input variables increases and there are no general solutions to keep their size small, nor to foresee their explosive growth. After reduction (and variable reordering [10]) the only way of further simplifying ADDs is by approximating the discrete functions they represent. One of the main strengths of our approach is that it enables effective approximations to achieve a good trade-off between accuracy and complexity. This is shown in the next section.

3 Approximation criteria and algorithms

The effectiveness of any approximation criterion depends on the representation of the function to be approximated. Consider the expressions at the two sides of Eq. (4) as equivalent models for the switching capacitance. At the right-hand side $C$ is expressed in terms of $N$ Boolean functions ($g_i$) and the model consists of $N$ BDDs. To cope with complexity, some BDDs may need to be simplified by approximating the corresponding functions. However, due to the involved dependence of $C$ on those functions, the error induced on $C$ by the approximation is almost unpredictable.

On the contrary, at the left-hand side of Eq. (4) the switching capacitance is directly represented as a discrete function and the model consists of a single ADD. To reduce the model complexity, approximation criteria can be directly applied to the target function, thus keeping the induced error under control. This is exactly what we do, working directly on the representation of $C(x^i, x_f)$.

The simplest way of simplifying an ADD is by means of node collapsing, that consists of reducing a sub-ADD to a single leaf node. Fig. 3.a shows the complete ADD of the switching capacitance of our example unit. Fig. 3.b shows a smaller ADD obtained by replacing the sub-tree rooted in node $n$ with leaf node 7.5. Since three nodes have been replaced by one, the overall size of the ADD has been reduced by 2 at the cost of losing some pattern dependence.

Example 3 Consider the ADD of Fig. 4.a. The sub-ADD rooted in node $n$ represents the dependence of $C$ on the second input vector ($x_f^i$) when the first one is $x^i = 00$. In particular, the switching capacitance is 0 if $x_f^i = 00$, while it is equal to $10\, \mu F$ in all other cases. This pattern dependence is lost in the ADD of Fig. 4.b when $x^i = 00$, the approximated value of $C$ is 7.5 regardless of $x_f^i$.

Without going through the algorithmic details of node collapsing, we remark that several sub-trees can be independently collapsed during a traversal of the original ADD. The overall cost of the process is linear in the number of nodes. Any trade-off between accuracy and complexity can be explored just by changing the degree of compression, i.e., the percentage of nodes to be collapsed. If no node is removed, the ADD represents the switching capacitance without approximations (the model has the accuracy of a gate-level simulation). If the entire ADD is collapsed in a single leaf, the model degenerates in a constant estimator.

More sophisticated algorithms can be conceived for ADD simplification. In this paper we only focus on node collapsing because of two main reasons: i) it is performed in linear time and ii) it is flexible enough to implement different approximation strategies.

In Ex. 3 we didn’t mention why node $n$ was chosen for collapsing and why the resulting leaf node was 7.5. We call approximation strategy a criterion to select the sub-ADDs to be collapsed and the values to be associated with

![Figure 4:](image-url)
the resulting leaf-nodes. For a given degree of compression, both the scope and the accuracy of the final approximation depend on the strategy adopted to steer the simplification procedure.

Since node collapsing always replaces a sub-function with a constant value, a general criterion to reduce the approximation error (and the loss of pattern dependence) consists of selecting for replacement sub-ADDs with minimum variance. The variance of an ADD is the variance of the function it represents. For a generic function \( f(x) \) of \( n \) Boolean variables

\[
\text{var}(f(x)) = \frac{1}{2^n} \sum_{x} (f(x) - \text{avg}(f(x)))^2
\]

where \( \text{avg}(f(x)) \) is the average value of \( f \):

\[
\text{avg}(f(x)) = \frac{1}{2^n} \sum_{x} f(x)
\]

To chose the target nodes for collapsing we need to compute the variance of all discrete functions associated with internal nodes. This can be done in linear time during a traversal of the ADD, using a recursive formula. Since leaves represent constant functions, for a generic leaf node \( k \) we have \( \text{var}(k) = 0 \) and \( \text{avg}(k) = \text{value}(k) \). For a generic internal node \( n \), both \( \text{var}(n) \) and \( \text{avg}(n) \) can be computed from those of its left and right children (denoted by \( n_{\text{left}} \) and \( n_{\text{right}} \), respectively):

\[
\text{avg}(n) = \frac{1}{2} \left( \text{avg}(n_{\text{left}}) + \text{avg}(n_{\text{right}}) \right)
\]

\[
\text{var}(n) = \frac{1}{2} \left( \text{var}(n_{\text{left}}) + \text{var}(n_{\text{right}}) - \text{avg}(n)^2 \right)
\]

Once \( \text{var}(n) \) has been computed for all nodes in the ADD, sub-ADDs rooted at nodes with minimum variance are chosen for collapsing. Node collapsing proceeds (possibly involving nodes with larger variance) until the global ADD is reduced under a target size. The overall process has the complexity of two ADD traversals.

Constant values used for replacement depend on the scope of the model. If we are targeting high accuracy on average power estimates, the average values computed for each original node \( \text{avg}(n) \) can directly be used to replace the corresponding sub-trees. In this case, \( \text{var}(n) \) represents the mean square error (mse) of the approximated sub-function.

**Example 4** Consider the ADD of Fig. 4a and assume that we need to reduce its size with a minimum impact on its average accuracy. During a first traversal of the ADD, the average value and the variance are computed for each internal node. Consider, for instance, node \( n \). According to Eq. (8), \( \text{avg}(n) \) and \( \text{var}(n) \) are given by:

\[
\text{avg}(n) = \frac{1}{2} (10 + 5) = 7.5
\]

\[
\text{var}(n) = \frac{1}{2} (25 + (5 - 7.5)^2 + 0 + (10 - 7.5)^2) = 18.75
\]

In Fig. 4a, \( \text{avg} \) and \( \text{var} \) are reported for some of the internal nodes. Node \( n \) is the one with the smallest variance. Hence, it is the replaced by a constant leaf node having value \( \text{avg}(n) \). The resulting ADD is shown in Fig. 4b.

The strategy adopted to obtain pattern-dependent upper bounds is slightly different. First, maximum values have to be used to replace sub-ADDs. Second, the variance does not represent any longer the mse caused by the approximation. Maximum values can be easily computed during the ADD traversal. For any leaf node \( k \), \( \text{max}(k) = \text{value}(k) \), while for any internal node \( n \), \( \text{max}(n) = \max(\text{max}(n_{\text{left}}), \text{max}(n_{\text{right}})) \). As for the mse, the following relation holds for each node:

\[
\text{mse}(n) = \text{var}(n) + (\text{max}(n) - \text{avg}(n))^2
\]

**Example 5** Our example ADD is reported again in Fig. 5a. Suppose that we need to reduce the size of the ADD making only conservative approximations. \( \text{avg}, \text{var}, \text{max} \) and \( \text{mse} \) are initially computed for each internal node. For node \( n \), \( \text{max}(n) = \max(10, 10) = 10 \), while \( \text{mse}(n) = 18.75 + (10 - 7.5)^2 = 25.5 \). Maximum value and mse are reported in Fig. 5a for some internal nodes. Nodes with minimum mse are then selected for collapsing and their sub-ADDs replaced by maximum-value leaves. In our example, node \( n \) is the best choice. The ADD after collapsing is shown in Fig. 5b.


3.1 Process flow

Approximations can be performed at any time during the construction of the ADD of the switching capacitance. This is due to the iterative implementation of Eq. (4). The pseudo-code of the main loop is reported in Fig. 6. At each step, the contribution of a new gate is computed and added to the overall function \( C \). Both \( C \) and its partial contributions (denoted by \( \delta^iC \) in Fig. 6) are represented by ADDs. Whenever the size of an ADD exceeds the maximum allowed value (MAX) the approximation routine is called to bring its size back under the limit. Since the function to be approximated is always a switching capacitance, the error induced to the model can be always controlled. Moreover, since the only operator possibly applied to ADDs after node collapsing is the arithmetic addition (\( \text{add}_{\text{sum}} \)), the same strategy may be used for local and global approximations. The respect of the global strategy is guaranteed by the following properties: \( \text{avg}(a) + \text{avg}(b) = \text{avg}(a + b) \) and \( \text{max}(a) + \text{max}(b) \geq \text{max}(a + b) \), that hold for any pair of discrete functions \( a \) and \( b \).

4 Experimental results

The algorithms described in this paper were implemented in C using the CUDD package for symbolic manipulation of Boolean and discrete functions [11]. Experiments were run on benchmark circuits from the MCNC suite [12]. Gate-level netlists were obtained by mapping the circuits on a test gate library. Input capacitances of fan-out gates were used as load capacitances for the driving ones.

We report the results of three sets of experiments. The first one is a case study (based on benchmark circuit cm85) aimed at exploring the modeling trade-off enabled by our approach. The second and third ones are extensive tests performed on several benchmarks to evaluate the accuracy achieved on average power estimates and the effectiveness of pattern-dependent upper bounds, respectively.

Two characterization-based power models are used for comparison: a constant average estimator (denoted by \( \text{cen} \)) and a linear model (denoted by \( \text{Lin} \)). \( \text{Lin} \) expresses power consumption as a linear function of input transitions: \( P = c_0 + c_1a_1 + \ldots + c_Na_N \), where \( a_i = x_i^j \oplus x_i^{j+1} \) and \( c_j \) are fitting coefficients. For each benchmark, both models were characterized to fit the results of a zero-delay gate-level simulation performed with a random input sequence with 0.5 average signal and transition probabilities.

We use the average signal probability (\( sp \)) and the average transition probability (\( st \)) to represent input statistics. For each model, the relative error on average power estimates is a function \( RE(sp, st) \). To evaluate \( RE(sp, st) \) we repeatedly ran concurrent RTL and gate-level simulations with random sequences of 10000 input vectors with different values of \( sp \) and \( st \).

For benchmark circuit cm85, \( RE \) is plotted in Fig. 7.a as a function of \( st \) (for \( sp = 0.5 \)). The strong dependence on input statistics is evident for both \( \text{Lin} \) and \( \text{cen} \) while their in-sample error is below 10\% (for \( st \) around 0.5), the out-of-sample error is much higher and it becomes larger than 100\% when \( st < 0.2 \). In contrast, the accuracy achieved by our model is almost independent of \( st \), as shown in Fig. 7.a by the solid-line curve labeled ADD. Incidentally, we remark that an upper bound of 500 ADD nodes was used during the construction of the model. The unbounded model would have more than 10000 nodes and it would fit exactly the results of gate-level simulations regardless of input statistics (i.e., \( RE(sp, st) = 0 \) for \( sp, st \)).

We call average relative error (\( ARE \)) the average value of \( RE(sp, st) \) over all simulation runs and we use it to represent the quality of RTL power models in terms of accuracy and robustness. For benchmark circuit cm85, we obtained \( ARE = 513.7\% \) for \( \text{cen} \), \( ARE = 195.2\% \) for \( \text{Lin} \) and \( ARE = 5.7\% \) for ADD.

The approximations described in Section 3 provide a wide range of trade-offs between the quality and the size of the RTL power models. Fig. 7.b shows the \( ARE \) of ADD-based power models of different sizes for cm85. Though the exact representation of \( C(x^r, x^d) \) would require an ADD with more than 10000 nodes, it is worth noting that ADDs with 10 or 5 nodes are sufficient to achieve power estimates with \( ARE \) below 20\% (i.e., one order of magnitude smaller than the \( ARE \) of a linear model with 12 fitting coefficients).

Experimental results on benchmark circuits are reported in Table 1. The name of the circuit, the number of inputs \( (n) \) and the number of gates \( (N) \) are reported in the first three columns. Columns four to eight refer to average power estimations. The \( AREs \) provided by constant (\( \text{cen} \)) and linear (\( \text{Lin} \)) estimators are reported in columns four and five for comparison. The \( ARE \) of our analytical model (ADD) is reported in column six. It is around 10 times smaller than that of linear estimators and 50 times smaller than that of constant ones. The constraint on the maximum number of ADD nodes (\( MAX \)) used during the construction of the model is shown in column seven. The general criterion used for choosing the value of \( MAX \) was that of making the size of the power model for a unit comparable with that of its functional description. The CPU time (in seconds) spent for building the model on a SUN Ultra Sparc 2 is reported in column eight.

The last four columns of Table 1 refer to conservative upper bounds of power consumption. Results are reported in terms of average relative error on maximum power estimates. For each simulation run, the maximum value provided by the upper bound was compared with the maximum value provided by gate-level simulation and the relative error (\( RE \)) was computed. As for the average power estimates, the \( ARE \) was evaluated as the average of \( RE \) over several simulation runs with different input statistics. Columns nine and ten report the average error made by a
constant maximum estimator (Con) and by our pattern-dependent upper bound (ADD), respectively. As a constant estimator we used the maximum value of the pattern-dependent upper bound. No linear models were used for comparison since they do not provide conservative bounds. The ARE of the constant estimator is always much larger than 100%, while the error made by ADD is always smaller than 60%. Moreover, pattern-dependent upper bounds of several units can be effectively composed to provide significant upper bounds for complex systems described at the RT level. The maximum allowed ADD size and the CPU time are reported in the last two columns.

For some circuits (e.g., C6288) ADDs with more than 100,000 nodes were required to bring the ARE below 30%. This is an inherent limitation of the ADD-based representation, whose complexity strongly depends on the functional and structural properties of the circuit. Though our approximation strategy can in principle be used to keep ADDs as small as desired, when the approximation becomes too aggressive it may lead to large errors, comparable to those of traditional RTL models. Overcoming this limitation is the target of our on-going work.

### 5 Conclusions

RTL power models based on characterization have two main drawbacks: i) their accuracy strongly depends on the input statistics, and ii) they do not provide worst-case information.

To overcome these limitations we have presented an analytical approach that does not require characterization. The power consumption of a combinational macro is expressed in terms of its internal switching capacitance. A pattern-dependent RTL model for the switching capacitance of the macro is automatically constructed during a traversal of its gate-level netlist. Since only structural information is exploited, the accuracy of the model does not depend on input statistics. Several approximation criteria can be applied during model construction in order to trade off accuracy for complexity. In particular, conservative approximations can be used to provide reliable pattern-dependent upper bounds.

We have presented the key ideas, outlined the main algorithms and discussed the experimental results obtained on benchmark circuits. In average, analytical models provide power estimates with relative errors more than 10^2 times smaller than those provided by pre-characterized constant and linear estimators.

### References


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**Table 1:** Experimental results.

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<th>Benchmark circuit</th>
<th>Average estimators</th>
<th>Upper bounds</th>
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