Erik Jan Marinissen, Philips Research Laboratories

Designers increasingly make use of large reusable modules, the so-called "cores", in order to efficiently use design resources and improve on time-to-market. To prevent testing from becoming the bottleneck in the entire development trajectory, the test community has set its hopes on the reuse paradigm as well. The potential benefits of design and test reuse w.r.t. time-to-market are obvious. However, many practical cases have demonstrated that design and test reuse might even increase development time if no special measures are taken to facilitate reuse. Additional features should enable "plug & play" in both design and test, and the costs of those features in terms of silicon area, performance degradation, power dissipation, etc. should be balanced against the benefits of reduced time-to-market.

Core-based design and test divide the IC development community into two groups: (1) core providers and (2) core users. To allow "mix & match" of cores from different sources standardization is needed. A core test standard should enable the integration of cores with different, possibly incompatible, core-internal tests onto one IC. Large semiconductor companies have internal core providers and core users; here, company-internal standardization is a solution. As an example, Philips has both design-for-test guidelines to ensure access to embedded cores, as well as CAD tools for test protocol expansion and scheduling in place. However, an industry-wide take off of core-based design requires an industry-wide standard w.r.t. core test, as pursued by IEEE P1500.

Industry-wide standardization is by definition slow and tedious. Fortunately, the P1500 Working Group has made good progress. Core providers, core users, and CAD companies will all benefit from one industry-wide standard as opposed to many different proprietary solutions. Therefore: let's make P1500 a success, it will be a key enabling factor for systems-on-chips!

Bruce Mathewson, Advanced RISC Machines Ltd.

As systems on a chip become increasingly complex it becomes more difficult to use a single test methodology for an entire system design. A number of different test methodologies exist and each has its own advantages and disadvantages. The following trade-offs must be balanced to determine the most suitable test approach to adopt:

- Fast / automated test vector generation
- High fault coverage
- Low silicon overhead
- Quick test time
- Ease of tracing faults from vector failures

With the increased size of silicon area available it becomes necessary to import IP blocks (or Virtual Components) from a number of different sources and it is possible that the test methodologies of the various components may not be compatible. Additional factors are also introduced into the choice of test methodology, such as:
- How the virtual component can be tested when it is not easily accessible from the device pins.
- How the virtual component can be integrated into the test process without revealing the internal IP.

In future the industry will require a standard approach to interface the test facilities of different virtual components, as well as a method of bringing the internal test interfaces to the external pins of the device.

Rudy Garcia, Schlumberger Technologies

In order to completely test manufactured system chips, we need to address all of the following requirements:
- VC Test - Each Virtual Component needs to be tested in situ, to the desired quality level.
- This requirement has further test implications:
  - Test Access - We need to access individual VCs from IC primary I/Os.
  - Test Isolation - That is, the need to be able to isolate one or more VCs from the rest of the chip for test purposes.
  - Interconnect Test - The ability to test the interconnect between VCs.
  - Shadow Logic Test - The system on a chip integrator generally adds user defined logic to the collection of VCs. The ability to test this logic which may not accessible from the primary I/Os is also required.
Test Vector Integration- How to allow for the integration of VC and User Defined Logic (UDL) into a single system-chip test program.

Test Logic Integration- What logic circuits may be necessary to manage the test logic in an efficient manner.

Failure Identification- Because the VCs may in general come from different providers, we need to have the ability of isolating failures to individual VCs.

Finally, although most of the above techniques suggest a structural test kind of methodology, recent experiments conducted by Sematech and published last year conclude that a purely structural test regimen is not sufficient to ensure the quality of outgoing devices. There continues to be a need for at-speed functional testing to ensure the quality of the product.

Yervant Zorian, LogicVision Inc.

Issues in testing core-based system-chips differ considerably from the conventional ASICs and standard ICs on a board. A core-based system-chip has only a single manufacturing and test instance for the whole system-chip. The individual cores need to have predetermined and autonomous test solutions, especially with today's trends of:

- Mixing distinct technologies on a single chip, such as DRAM, analog and logic technologies, hence the need for a single ATE based test solution.
- Mixing diverse levels of hardware descriptions on a single chip, such as layout, transistor, gate, RTL, etc., hence the need for self-contained test solution.
- Increasing the dominance of non-mergeable cores in today's system chips, by using providing hardened soft cores, hence the need for autonomous test.
- Increasing the internal speed of system-chips versus the external (I/O speed), hence the need for at-speed test based on-chip clocking.
- Increasing need for plug-n-play of cores from diverse sources, hence the need for self-contained test solutions.
- Requiring IP protection, hence the need of a test solution with limited structural accessibility.

The above trends force us to use embedded test resources in IP cores. A good example of such resources would be cores with full BIST capabilities or at least BIST-ready feature. The system-chip test strategy has to leverage such resources and build the overall test solution accordingly.

Sujit Dey, Univ. of California, San Diego

The key features that make system-on-chips using IP cores an attractive system design methodology, namely design re-use, heterogeneity, configurability, and customizability, are also the ones that make testing and debugging system-on-chips a complex challenge. Design re-use of IPs from various sources, and integration of heterogeneous components - from processor cores to complex multimedia cores, digital and analog components, synchronous and asynchronous interfaces, and electrical and mechanical components, pose serious challenges to testing a system chip, with diverse test strategies employed by the heterogeneous components. While development of test standards by the IEEE P1500 WG and the VSIA are necessary steps to ease the tasks of chip-level test access and test integration, new test methodologies need to be developed to address the following issues:

- Testability characterization of soft IPs,
- Test analysis tools to determine optimal chip-level test access structures, and test area and test time trade-offs,
- Test planning and scheduling tools at the chip-level,
- Debugging and diagnosing ICs which have significant software content,
- Testing mixed-signal ICs, and future microelectromechanical systems (MEMS) on silicon.

In the system-on-chip design paradigm, the processor core, the associated peripheral units, and the underlying bus, memory and communication architectures, can all be configured and customized to best match the embedded system application, thereby giving tremendous cost and performance advantages over traditional system-on-board approaches. How are we going to address the issue of standardization of test and access mechanisms, when the cores themselves can be customized, and the system chip configured, by the system designer? We need to rethink our "standard test interface" requirements, and evolve a flexible, and customizable, test re-use strategy. We definitely need standards for today's needs, but we also need new test methodologies and tools to cope with the multi-million gate, heterogeneous, and customizable system chips of tomorrow.

Rob Roy, Intel Corp.

No advance position statement.