PANEL: TECHNICAL CHALLENGES OF IP AND SYSTEM-ON-CHIP: 
THE ASIC VENDOR PERSPECTIVE

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Organizers: Andrew Graham – Silicon Integration Initiative, Austin, TX  
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Panelists: Bruce Beers – IBM, Essex Junction, VT  
Jeffery Hilbert – LSI Logic Corporation, Milpitas, CA  
Anand Naidu – Sand Microelectronics, Santa Clara, CA  
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SUMMARY

The vision of easily accessible IP that can be quickly integrated on silicon as "virtual components" is a compelling one, with deep implications for reuse methodology and EDA technology. Activities of the VSI Alliance, starting nearly two years ago, have fueled interest in IP and raised market expectations for value and reusability to very high levels. Indeed, the sheer number of new IP companies, in combination with third-party ASIC libraries and EDA tools offerings, suggests that the era of plug and play IP has arrived. Today, the claimed independence of IP from the underlying silicon has led to bold market claims for foundry manufactured system chips using internet sourced IP with Lego block, snap-together integration simplicity. Traditional roles of foundries, ASIC suppliers, and EDA vendors are blurring. To the end customer, the situation presents both opportunities and risks. Are we on the cusp of a new era, or a rude awakening?

From the perspective of leading ASIC vendors, the evolution of IP-based systems on silicon, along with the means and methods of producing them, are not new. Full use of rapidly-increasing raw ASIC gate counts – which is synonymous with systems on silicon – has been a driving force in the ASIC industry for many years. As developers of high-value IP and systems architectures, the leading ASIC companies have an established record of experience with design and system chip level integration. This experience – e.g., with system-level analysis, integration of cores designed to common bus-structures, etc. – can be leveraged toward practical realization of an IP vision that offers the silicon consumer more choice without unacceptable implementation risks. On the other hand, from the perspective of a pure IP integrator, IP is poised to change the way customers and ASIC vendors themselves produce systems-on-silicon, just as vendor-specific tools evolved to commercial CAE starting a decade ago. Early IP success stories are pointing the way to a new, more specialized business model where IP, tools, services, and silicon foundry are brought together based on the specific needs of a given project.

This panel will address technical challenges presented by the systems-chip opportunity, as well as practical expectations and key missing pieces of industry infrastructure. Such pieces include: customer expectations, EDA technology, standards, legal barriers and associated risks facing ASIC suppliers and EDA vendors, challenges of incorporating 3rd-party IP, and practical reuse methodologies. In this forum, a noteworthy challenge – which has remained constant throughout the evolution to deep-submicron – is the ability for customers to develop their systems when faced with a widening gap between process technology and commercial EDA tools. As silicon suppliers continue to focus on providing the industry with advanced technologies and products, EDA suppliers must also increase their focus on providing tools and infrastructure. Another example challenge, faced by ASIC vendors, lies in supplying the high-level core models required for emerging cycle-based simulators, and supporting the use of cores in emulators and accelerators, when no standards for model creation or protection exist. Standard model interfaces such as those that exist for event-based simulators must be developed to support cycle simulators, emulators, accelerators as well as hardware-software co-verification tools. The panel will also examine essential factors to consider in the use of IP, based on their experience with the latest silicon process technologies. Finally, the ASIC vendor participants will showcase their joint efforts to build an effective IP infrastructure for the industry.