Panel: User Experience with High Level Formal Verification

Convenors: Randy E Bryant - CMU, USA and Gerry Musgrave - Brunel University, UK

Formal Verification is a "hot topic" for the user and vendor community. It has moved from the research community to the industrial domain in a very short time. Everyone wants to know more about how effective the techniques are. This experienced user panel will attempt to address your concerns in an open and frank way. They will give their personal opinions and not the commercial hype that so often heralds a new era.

Formal verification methods is a generic term which currently covers equivalence checking, both structural and sequential, model checking and formal proof reasoning. To date only the first category has begun to be accepted as an adjunct to the verification process particularly at the gate level. Yet the higher levels of abstraction have the potential for greater fertility from use of the other classifications of formal tools.

Leading edge industries are beginning to explore the value of the more sophisticated techniques. Often their learning curve has been via the structural equivalence checking route, which when operational in an ASIC division has valuable lessons for the user and CAD communities.

Higher level techniques would be those which ensure consistency of constraints such as, reset requirements, safety requirements, determinacy and other parameter factors across all levels of implementation. It moves this form of validation from the post design phase to the proactive design aid. This is a much bigger change in design philosophy compared to equivalence checking yet it is a long way from the purist view of formal verification. This latter approach requires a formal proof engine to validate all design decisions against a reasoned specification. Hence the road map for formal verification has just started and there is a long way to go. But the confidence expressed by the many vendor announcements indicates that this is a highway we will be travelling along.

The panel will address such questions as:

- How effective are these techniques in solving the simulation bottleneck?
- How easy is it to embed them in the existing design flow or do we have to change the design flow to gain maximum improvement in time-to-market?
- Is there a re-education requirement for the design community in order to benefit from these tools?
- How do we transform from using formal verification tools as a post design checking to become a proactive design aid in achieving quality designs in a shorter time?
- Are VHDL and VERILOG specifications adequate input to these design decision aids?
- Are these the tools that will give IP real credibility?

These and many more questions, mainly from the audience, will be put to our international panellists who have had experience in the field from a number of industry sectors.

The Panel:

Fumiyasu Hirose, Fujitsu, Japan
Michael Payer, Siemens Semiconductors, Germany
Pierre Aulagnier, Cisco, USA
Alan Silbert, Nortel, Canada
John Van Tassel, TI, USA

Chair G. Musgrave
Uxbridge, UK