As the electronics industry moves towards systems-on-a-chip goals, the design automation needs will rapidly increase far beyond what can be supported by today’s tool flows and design methodologies. Design reuse will be a pre-requisite in most cases, and software content is expected to exceed 50% to 70% of the functionality. Yet today we are still limited to very segmented hardware and software flows. Our HDL’s serve us well for HW implementation, but do not contain the robustness for true system-level description and analysis prior to partitioning in various implementation media (analog, digital, software, RF, optical, etc.). The time has come to embrace a more appropriate system design capability that suits our emerging system description and design needs.

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