Design of Nonlinear Switched-Current Circuits Using Building Block Approach

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Abstract — This paper studies a family of switched-current and current-mode building blocks for non-linear sampled-data signal processing and proposes several new switched-current nonlinear circuits which can be designed using the building block approach. The proposed circuits present merits of simple circuit configuration, low voltage and low cost. The development of these circuits has not only expanded the family of the state-of-the-art switched-current circuits but also provided high level macrocells for the design of complex SI signal processing systems.

I. INTRODUCTION

The switched-current (SI) technique [1] is a newly developed current-mode circuit design technique for analogue sampled-data signal processing. The SI advantages, such as the compatibility with standard digital CMOS processing technology and the capability of working with low supply voltage, make it more promising for application to the monolithic implementation of mixed analog and digital VLSI.

The application of the switched-current technique is originated from the linear frequency filtering at the early development stage. The synthesis methodology, basic building blocks and practical design considerations have been fully studied, developed and successfully applied to the SI filter design [1]. However, nonlinear applications of SI techniques have not yet attracted as much attention as the SI filters have. Recently only a few nonlinear SI circuits have been reported in the literature [2, 3].

Nonlinear applications of SI techniques are still in the infancy. Application areas and systematic design methodology are rarely reported. This paper proposes several new SI nonlinear circuits and attempts to develop a systematic approach to design them. In Section II, a family of switched-current and current-mode building blocks for nonlinear signal processing is presented. Based on the time division principle, three new switched-current nonlinear circuits, which can be designed using the above building blocks, are proposed in Section III. As an example, the time-division multiplier-divider is designed and simulated by SPICE in Section IV.

II. SWITCHED-CURRENT AND CURRENT-MODE BUILDING BLOCKS

A. Two input current comparator

A two-input current comparator (Comp in Fig.1) is the most common building block for nonlinear signal processing. It can be realized by a two-input current subtracter (Subtra) and a one-input transimpedance current comparator (Comp) as shown in Fig.1. The two-input current subtracter, performing function of \( i_o = i_p - i_n \), is realized using cascode current mirrors as shown in Fig.2. The one input transimpedance current comparator is the high speed and high resolution current steering comparator proposed by A. Rodriguez-Vazque [4]. This comparator can achieve resolution in pA and comparison speed in several ns.

B. Current Schmitt-trigger with external signal controlled hysteresis

In nonlinear signal processing, current Schmitt-trigger with controlled hysteresis is widely used. Usually the hysteresis value is controlled by a fixed reference current [5].

![Fig. 1. Two input current comparator.](image-url)
However, in some cases, the hysteresis should be controlled by a varying input signal. This section proposes such a new current Schmitt-trigger with external signal controlled hysteresis.

Shown in Fig.3 is the proposed current Schmitt-trigger. It is basically a two-input current comparator \textit{Comp} with its negative and positive input branch controlled by the logic state of the final output voltage $v_k$. The input signal $i_{in}$ is always directed to the positive input port of the \textit{Comp}. The hysteresis current $i_{hy}$ is directed to the positive or negative input port of the \textit{Comp} by alternatively turning on the two switch transistor $M_n$ and $M_p$ when voltage $v_k$ goes high or low.

The SPICE simulated hysteresis characteristics of this circuit is depicted in Fig.4 with an input current range from $-3\mu A$ to $+3\mu A$ and a hysteresis current $2\mu A$. Simulation shows that the comparison speed of this Schmitt-trigger is much the same as that of the current steering comparator [4]. Monte Carlo Analysis shows that the offset and resolution of this circuit are less than $1nA$ with a standard deviation of mismatches in length and width of $0.01\mu m$ in the mirrors.

C. Switched-current integrators

In order to tackle the charge-injection and channel length modulation problems in the second-generation switched-current integrators, a $S^2$I technique [6] and the cascode structure are employed respectively. A lossless inverting/non-inverting integrator (\textit{integ}) using the cascode two-step cell is designed as shown in Fig.5. It performs the following transfer function (Eqn.(1)) in the $z$-domain.

$$i_o(z) = \frac{a z^{-1}}{1 - z^{-1}} i_1(z) - \frac{a}{1 - z^{-1}} i_2(z) \quad (1)$$

Using the same cascode two-step cell, a damped inverting/non-inverting integrator (\textit{Dil}) is designed, as shown in Fig.6, which performs the transfer function given in Eqn.(2).

$$i_o(z) = \frac{a}{1 + \alpha_f z^{-1}} i_1(z) - \frac{a}{1 + \alpha_f z^{-1}} i_2(z) \quad (2)$$

Fig. 2. Two input current subtractor.

Fig. 3. Current Schmitt-trigger with external signal controlled hysteresis.

Fig. 4. Hysteresis characteristic of current Schmitt-trigger with external signal controlled hysteresis.

Fig. 5. Cascode two-step inverting/non-inverting lossless integrator.

Fig. 6. Cascode two-step damped inverting/non-inverting integrator.
III. SWITCHED-CURRENT NONLINEAR CIRCUITS

The SI technique for nonlinear signal processing is a rather new application area. The SI potential for nonlinear signal processing has not yet been fully exploited. On the contrary, the development of SC nonlinear applications is quite mature now. Since the SI circuits have many building blocks having the same functions as those of SC circuits, it would be very desirable if SI nonlinear circuits could be directly synthesized from the existing function diagrams of the SC circuits.

In this section, three new SI nonlinear circuits will be proposed based on the SC time-division principle. It is quite interesting that a SI pulse width modulator could be developed from a SC pulse-width modulator principle by employing SI basic building blocks described in the last section. From this SI pulse-width modulator, a current controlled oscillator and a time-division multiplier-divider can also be derived.

A. SWITCHED-CURRENT PULSE WIDTH MODULATOR

A pulse-width modulator is a very useful analog building block which can be used to realize time-division multiplier, multiplier-divider and current-controlled oscillator.

Shown in Fig. 7 is the diagram of a current-domain pulse width modulator (PWM) [7] which generates a quantized signal \( K \) that oscillates between two levels (high and low or 1 and -1) at the output of the comparator. The PWM is composed of two phase reversers, a non-inverting integrator with transfer function of \( H(z) = \frac{z}{a_3} \) and a two-input comparator whose positive port is connected to a scaled phase-reversible signal \( \pm a_3 z \). All the phase reversers are controlled by the rectangular waveform signal \( K \) so that during \( K = 1 \), the integrator is with input current of \(-a_1 y + a_2 z\) and the positive port of the comparator is connected to \( a_3 z\), while during \( K = -1 \), the same integrator is with input current of \(-a_1 y - a_2 z\) and the current to the positive port of the comparator is \(-a_3 z\).

We define that \( T_1 \) is the time duration during which \( K \) keeps value 1 in one cycle (when \( K = 1 \) and \( K = -1 \)) and \( T_2 \) is the time duration during which \( K \) keeps value -1. It can be proved that \( T_1 \) and \( T_2 \) are with value of

\[
T_1 = \frac{2a_3 z}{(-a_1 y + a_2 z) \alpha} \frac{T_c}{a} \quad \text{and} \quad T_2 = \frac{2a_3 z}{(a_1 y + a_2 z) \alpha} \frac{T_c}{a}
\]

where \( 1/T_c \) is the sampling frequency of the integrator.

It is clear that the output \( K \) of PWM is a pulse train with \( T_1 \) and \( T_2 \) as the width of the positive and negative portions of the pulses. The frequency of the pulse \( K \) is

\[
f_k = \frac{1}{T_1 + T_2} = \frac{a_3}{4a_3} \left( 1 - \frac{a_1 y}{a_2 z} \right) \frac{\alpha}{T_c}
\]  

(3)

The above pulse width modulator can be realized by SI technique using the building blocks presented in the last section. The comparator with one input port controlled by a phase reverser can be implemented by a current Schmitt-trigger with external signal controlled hysteresis. The integrator with phase-reversible input can also be realized by a non-inverting/inverting integrator with its input controlled by two switches. The SI pulse width modulator is shown in Fig. 8.

B. SWITCHED-CURRENT MULTIPLIER-DIVIDER

A time-division multiplier-divider, as shown in Fig. 9, can be realized simply by adding a pulse amplitude modulator to the above pulse-width modulator. The amplitude of the pulse train \( K \) is modulated by input signal \( x \). When \( K = 1 \), a value of \(+x\) is fed forward to the low pass filter (LPF) with gain of value \( b \), while \(-x\) is fed when \( K = -1 \). The output of the LPF, which is also the average value of the modulated pulse train, is given in Eqn.(4). It is the desired multiplication of signal \( x \) and \( y \), divided by signal \( z \).

\[
i_o = b \frac{T_1 - T_2}{T_1 + T_2} x = b \frac{a_1 y}{a_2 z}
\]  

(4)

A much simplified multiplier-divider based on the same time-division principle will be given in Section IV as a design example to show the SI potential for nonlinear signal processing.

![Fig. 7. Block diagram of pulse width modulator.](image1)

![Fig. 8. Switched-current pulse width modulator.](image2)

![Fig. 9. Diagram of time-division multiplier-divider.](image3)
C. Switched-current current-controlled oscillator

It is quite interesting that the pulse width modulator described in Section IIIA can realize a current-controlled oscillator by removing the $a_{i}y$ input branch from Fig.8 and substituting input $a_{3}z$ with a fixed hysteresis current $I_{by}$ and $a_{3}z$ with a controlling current $I_{con}$. The resulting SI current controlled oscillator is shown in Fig.10 which is similar to that proposed by Raahemi [3].

The oscillator gives a triangular current wave with maximum value of $I_{by}$ and minimum value of $-I_{by}$ at the output of the integrator. By applying the analysis procedure used in Section III.A, the oscillation frequency of the current-controlled oscillator is given by Eqs.(5). The oscillation frequency depends linearly on $I_{con}$. It is also determined by the hysteresis of the Schmitt-trigger and the parameters of the SI integrator, e.g., the switching frequency $(1/T_{c})$ and the transistor aspect ratio ($a$).

$$T_{1} = T_{2} = \frac{2I_{by} T_{c}}{I_{con} a} \quad \text{and} \quad f_{o} = \frac{1}{T_{1} + T_{2}} = \frac{\alpha}{4} \frac{I_{con}}{I_{by}}$$ (5)

SPICE simulation has been done under supply voltage of ±3V and design parameters $\alpha = 0.1, I_{by} = 25\mu A, f_{c} = 2MHz$. Fig.11 depicts the oscillation frequency of the SI current-controlled oscillator. It can be seen that the oscillation frequency is linearly proportional to the controlling current $I_{con}$.

![Fig. 11. SPICE simulated oscillation frequency vs. reference current](image)

IV. DESIGN EXAMPLE: TIME-DIVISION MULTIPLIER-DIVIDER

To our knowledge, a switched-current multiplier-divider has not been reported previously. The one proposed in this paper is the first multiplier-divider designed using switched-current techniques.

A. Block diagram and operating principle

Shown in Fig.12 is the simplified block diagram of a SC time-division multiplier-divider proposed by Chichi [8]. In this section we use SI techniques to implement this principle and propose a SI time-division multiplier-divider.

A practical realization of a SI multiplier-divider based on the above principle is presented in Fig.13. The circuit consists of SI building blocks, i.e., two SI damped integrator, a Schmitt-trigger with external signal controlled hysteresis.

The damped SI integrators (DI1 and DI2) shown in Fig.13 have been described in Fig.6, which have z-domain transfer functions of the form

$$H_{i}(z) = \begin{cases} \frac{-a_{i}}{1-k_{i}z^{-1}} & \text{for } v_{k} = -1 \\ \frac{a_{i}}{1+k_{i}z^{-1}} & \text{for } v_{k} = 1 \end{cases}$$ (6)

where

$$a_{i} = \frac{a_{i}}{1+a_{f_{i}}}, k_{i} = \frac{1}{1+a_{f_{i}}}, i = 1, 2.$$ 

Hence, the circuit shown in Fig.13 can be described by
the following set of difference equations

\[ i_x(n) = \begin{cases} b_1 i_x(n-1) + a_1 i_y(n-1) & \text{for } v_k = 1 \\ b_1 i_x(n-1) - a_1 i_y(n) & \text{for } v_k = -1 \end{cases} \]

\[ i_m(n) = \begin{cases} b_2 i_m(n-1) + a_2 i_x(n-1) & \text{for } v_k = 1 \\ b_2 i_m(n-1) - a_2 i_x(n) & \text{for } v_k = -1 \end{cases} \]

(7)

(8)

The above set of difference equations can be solved by applying the similar procedure given in [8]. The mean value and the oscillation amplitude of output signal \( i_o \) can be proven to be

\[ i_o = \frac{a_1 i_x i_y}{a_2 i_x} \quad \text{and} \quad \Delta i_o = \frac{a_1}{a_2} \delta i_y \]

(9)

provided that the following conditions hold:

1. \( 0 < f_k < f_c - \left| \frac{a_2}{a_1} \right| i_x \pm i_x \right| = \delta i_x, (i_x > 0) \)

2. \( a_{f1} = a_{f2} < 1 \)

where \( f_k \) (Eqn.(10)) is the frequency of the output signal \( v_k \) and \( f_c \) is the sampling frequency of the damped integrator.

\[ f_k = -\frac{a_2}{a_1} f_c \ln \frac{b_2}{4\delta} \left[ 1 - \left( \frac{a_2}{a_1} \right)^2 \right] \]

(10)

B. SI implementations and simulations

The building blocks employed in the block diagram of Fig.13, such as the SI damped inverting/non-inverting integrator, current Schmitt-trigger with external signal controlled hysteresis and current mirrors can be realized using the building blocks introduced in Section II. In actual circuit design, the amplification parameters are chosen as \( a_1 = a_2 = a_{f1} = a_{f2} = 0.04 \) and \( \delta = 0.02 \). Since both signal \( i_x \) and \( \delta i_x \) are simultaneously used in the block diagram of Fig.13, this can be achieved by mirroring input current signal \( i_x \) into \( i_x \), \( -i_x \), and \( \delta i_x \). The power supply is \( \pm 3V \) and the two phase non-overlapping clock frequency \( (\phi_1, \phi_2) \) covered the interval from \( 5kHz \) to \( 15MHz \).

The multiplier-divider has been simulated by SPICE with \( 1\mu m \) CMOS process technology. Fig.14 depicts the DC multiplication characteristic of the multiplier-divider when the output signal is taken as a function of \( i_x \) while \( i_x \) is used as a parameter and \( i_x \) is kept constant at \( -30\mu A \) (i.e., \( i_x = 30\mu A \)). The DC division characteristic (Fig.15) is also obtained when the output signal is measured as a function of the signal \( i_x \) while the DC signal \( i_y \) is used as the parameter and \( i_x \) is kept constant at \( 4\mu A \). In both cases the clock frequency of the SI damped integrator is \( f_c = 200kHz \). Fig.16 shows the multiplication of a sine wave \( i_x \) (with frequency of \( 1kHz \) and amplitude \( 10\mu A \)) and a cosine wave \( i_x \) (with the same frequency of \( 1kHz \) and amplitude \( 20\mu A \)). \( i_x \) is kept constant at \( -20\mu A \).

The above DC and AC simulation results have shown that the proposed switched current time division multiplier-divider can correctly perform the four quadratic multiplication of two DC or AC signals of \( i_x \) and \( i_x \). The division function is correct when the input current \( i_x \) is always negative (i.e., \( i_x \) is positive). Since the precision of the multiplier-divider depends on the match of the two damped integrators, for a standard \( 0.01\mu m \) mismatch of transistors dimension (both width and length) between the two damped integrators, simulation under clock frequency of \( 15MHz \) has shown that the multiplier-divider could achieve total error less than \( 0.08\% \) for the input currents with amplitude less than \( 50\mu A \).

Table I compares the performance of the SI multiplier-divider with the SC counterpart[8]. It can be seen that the proposed SI multiplier-divider presents the following merits.

1. The bandwidth of the SI multiplier-divider is higher than its SC counterpart. This is because the additional capacitors and high impedance nodes in the SI circuit do not exist in the SC circuit.

2. The SI multiplier-divider can work with low supply voltage. In our design, a supply voltage with value of \( \pm 3V \) is chosen. In fact even lower supply voltage...
Multiplication of a sine wave $i_x$ and a cosine wave $i_y$.

![Figure 16](image_url)

**TABLE I**

| Performance of SI multiplier-divider (MD) compared with that of the SC counterpart. |
|----------------------------------------|-------------------------------------------------|
| **Bandwidth** | SI MD | SC MD |
| Supply voltage | 700kHz | 300kHz |
| Transistor numbers | small | large |
| CMOS Technology | pure digital | double poly |

could also be employed according to the requirements of actual circuits.

3. The SI multiplier-divider consumes smaller number of MOS transistors, thus occupies smaller chip area than the SC counterpart.

4. In the SI implementation, there is no need for the linear capacitor as those in the SC counterpart. So pure digital CMOS process technology could be used to fabricate the SI multiplier-divider. Thus fabrication cost is greatly reduced, especially when the SI circuit will cohabit with some digital circuitry in a single chip.

5. The proposed SI multiplier-divider is suitable for constructing of many signal processing circuits and devices, e.g., correlators, convolvers, adaptive filters, and curve fitting generators. It could also be applied to modulation, detection, frequency translation, automatic gain controlling, squaring, and square rooting of signals.

**V. Conclusions**

The application of switched-current (SI) techniques for nonlinear sampled-data signal processing is a rather new application area compared with the SI frequency domain linear filtering applications. This paper has presented some switched-current and current-mode build-

**References**


