Timing Analysis and Optimization: From Devices to Systems

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ABSTRACT

Timing analysis spans the entire design process from RTL synthesis to timing sign-off including schematic design, logic synthesis, floor plan, place and route, clock distribution etc.

In this embedded tutorial we will cover timing analysis from devices to systems. At the transistor level we will cover static, dynamic and interconnect analysis. At the gate level we will cover path analysis including false paths and static and dynamic sensitization aspects. The new Delay Calculator Language (DCL) will also be covered. We will tie the statistical properties at each level to put them under proper perspective.