A CMOS smart image sensor LSI for focal-plane compression

Shoji Kawahito, Makoto Yoshida, Masaaki Sasaki
Daisuke Miyazaki, Yoshiaki Tadokoro
Department of Information and Computer Sciences
Toyohashi University of Technology
Toyohashi 441
Tel: +81-532-44-6755
Fax: +81-532-44-6757
e-mail: kawahito@signal.tut.ac.jp

Kenji Murata, Shiro Doushou
Akira Matsuzawa
Advanced LSI Development Center
Matsushita Electric Industrial Co. Ltd.
Moriguchi 570
Tel: +81-6-906-4906
Fax: +81-6-906-3851
e-mail: matsu@vhlse.kiel.co.jp

Abstract—
A CMOS smart image sensor LSI with video compression is presented. The proposed on-sensor compression scheme using an analog 2-D DCT processor is particularly useful to achieve low-power one-chip digital camera. A prototype image sensor LSI has been developed using 0.35um double polysilicon, triple metal CMOS technology. Image coding using the implemented LSI has been demonstrated.

I. INTRODUCTION

Recent progress in mobile terminals strongly urges us to develop a low-power, low-cost, small digital video camera to treat moving pictures on it[1]. However, the present digital video camera does not meet these requirements, especially on the power dissipation, because of the large power consumed by video encoders.

In this paper, a CMOS image sensor integrating video compression using intraframe coding is presented. The CMOS sensor has a block (8 x 8) access function, and the image is directly encoded by an analog 2-D DCT processor. Analog 2-D DCT coefficients are digitized based on an adaptive technique. The proposed scheme greatly reduces the total power required for video compression.

II. ARCHITECTURE

Figure 1 shows the block diagram of the CMOS image sensor with focal-plane image compression[2]. The compression is based on intra-frame coding using 8 x 8-point 2-D DCT. The final output can be compatible to the motion JPEG standard. In the conventional digital camera systems, the total power consumed by CCD image sensor, the off-chip analog front-end processor and the frame buffer memory becomes more than 1W. In the proposed scheme, the CMOS image sensing array itself consumes low power compared to CCD. The image sensing array has a block access function where a unit of 8 x 8 pixels is read out directly. This block access scheme eliminates the frame buffer memory and the related hardware and eliminates the power consumed by them.

![Fig. 1 CMOS image sensor with video compression](image_url)

The analog 2-D DCT processor directly computes the 2-D DCT of the 8 x 8 pixel block read out from the imager array. The 2-D DCT of 8 x 8-size data, \( Y = CX A \) is calculated by \( G = CX \) and \( Y^2 = CG^2 \), where \( C \) is a cosine kernel matrix, and \( G \) is an intermediate matrix. The basic operation of the 2-D DCT is a weighted summation of input image signals using fixed coefficients, allowing to realize the analog implementation of the 2-D DCT. The analog 2-D DCT processor consists of 1-D DCT circuits, an analog memory and a timing controller. A column of 8 pixels is given to the 1-D DCT processor for 8 times, and the intermediate results are stored in 8 x 8 cell memory. After transposing the memory data, the data is given to the 1-D DCT again, and thus the 2-D DCT coefficients are obtained. Using two 2-D DCT cores as shown in Fig. 1, the throughput can be doubled. The total steps to calculate 2-D DCT is only 16. Because of this high throughput, the analog 2-D DCT processor consumes low power. Fig.2 shows the analog 1-D DCT processor based on switched capacitor (SC) circuits. 32 additions and 32 multiplications are performed in parallel. The basic SC cell is composed of 2 capacitors and several switch transistors. The coefficient is given by the ratio of a coefficient capacitor to a feedback capacitor of opamps. The unit capacitance is chosen as 0.5pF.

In the proposed scheme, the 2-D DCT coefficients are digitized by an adaptive A/D converter. In this case,
only small number of 2-D DCT coefficients has to be digitized by a high-resolution A/D converter, and others are digitized by a low-resolution A/D converter. The adaptive A/D conversion technique using A/D converter cores with two kinds of resolution allows us to achieve totally low power in video A/D converter, because the sampling frequency of the high-resolution A/D converter can be greatly reduced.

![Fig. 2 1-D DCT circuits.](image)

III. IMPLEMENTATION AND EXPERIMENTAL RESULTS

We have designed and implemented an essential part of Fig.1. Fig. 3 shows the photomicrograph of the implemented chip which consists of a 128 x 128-pixel block-access CMOS imager and an analog 2-D DCT processor. The chip is fabricated with 0.35μm triple-metal double-poly-silicon n-well CMOS technology. The chip size is 4.36 x 4.36mm². Fig 5 (a) and (b) show the image captured by the implemented CMOS imager and the reconstructed image using the analog 2-D DCT processor at 30 frame/s, respectively. Both imager and 2-D DCT outputs of the LSI are digitized using 8-channel 10-bit A/D converter, stored in frame buffer memory, and then loaded into the computer. The inverse 2-D DCT is performed by software in the computer, and finally a reconstructed image is obtained. The PSNR of 36.7dB in the reconstructed image is obtained. This demonstrates for the first time that the analog approach in 2-D DCT can be actually used in image encoding.

The compression ratio using the proposed smart CMOS image sensor is more than 10 at PSNR of 34dB. The power including CMOS imager and the analog 2-D DCT processor is less than 20mW, and the total power of the overall system of Fig. 1 is estimated to be less than 50mW, allowing to use for personal mobile computers and telephones.

![Fig. 3 Implemented CMOS image sensor chip.](image)

![Fig. 4 Images captured and reconstructed.](image)

IV. SUMMARY

The CMOS image sensor integrating video compression is particular useful for personal mobile products, because of the low power and the compactness. On-sensor motion vector estimation is one of important topics in the low power design of video compression hardware based on MPEG2 standards.

REFERENCES
