Power-Pro: Programmable Power Management Architecture

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Abstract—This paper presents Power-Pro architecture (Programmable Power Management Architecture), a novel processor architecture for power reduction. Power-Pro architecture has following two functionalities, (i) Supply voltage and clock frequency can be dynamically varied, (ii) Active data-path width can be dynamically adjusted to requirement of application programs. For the application programs which require less performance or less data-path width, Power-Pro architecture realize dramatic power reduction.

I. INTRODUCTION

With recent popularizations in portable, battery-powered devices such as digital cellular telephones and personal digital assistants, minimizing power consumption of VLSI circuits becomes more important. As the system level power reduction techniques, the choice of optimal supply voltage ($V_{DD}$) and optimal active data-path width have strong impacts. In this paper we propose novel processor architecture Power-Pro [2] which can vary $V_{DD}$ and active data-path width of processor by its own instruction. Power consumption for the processing of the programs can be dramatically reduced by optimizing the $V_{DD}$ and active data-path width for each application programs.

We designed and fabricated a single pipeline processor which equips functionality of Power-Pro architecture to make clear the effect of power reduction of Power-Pro architecture.

II. ARCHITECTURE

A. The scheme of dynamic $V_{DD}$ scaling

The power dissipation in a digital CMOS circuit is in proportion to square of the $V_{DD}$. Therefore, reduction of the $V_{DD}$ is very effective for power reduction[1]. But reducing power supply voltage causes increase of circuit delay. Because of this power-delay trade-off in CMOS circuits, obtaining high performance with low power consumption is difficult. Power-Pro architecture as shown in Fig. 1 can optimize power-delay trade-off by scaling the $V_{DD}$ dynamically. We can define the scheme of dynamic $V_{DD}$ scaling as follows.

- The architecture has a special instruction by which $V_{DD}$ can be set and has power control register which save a $V_{DD}$ level.

- The architecture has a variable clock scheme by which clock frequency closely match with chip’s delay even when the $V_{DD}$ is varied.

![Fig. 1. Programmable $V_{DD}$ Control](image)

Power-Pro architecture needs a support of the power converter such as DC-DC converter or PLL[3, 4]. However, actual design of on-chip DC-DC converter is our future work. For the evaluation of Power-Pro architecture, we implemented an off-chip DC-DC converter.

B. The Scheme of Dynamic Data-path Width Scaling

We can define the scheme of dynamic data-path width scaling as follows.

- Each instruction can specify not only operation but also active data-path width.

- Some part of data-path can be stopped by gated clocks according to the instruction.
If an application program which has only 8-bit type variables are processed by 32-bit microprocessor, invalidate the 24 bits of data-path reduces power consumed by clock terminal of register and data bus as shown in Fig. 2.

![Fig. 2. Programmable Data-path Width Control](image)

### III. Characteristics and Simulation Results

We designed and fabricated a **Power-Pro** which equips minimal functionalities of Power-Pro architecture, and its microscopic photograph is shown in Figure 3. We joined VDEC(VLSI Design and Education Center) pilot chip project so as to implement an actual chip. The **Power-Pro** is a 32-bit RISC microprocessor with five pipeline stages.

We used VHDL for logic design, Synopsys tools for logic synthesis and simulation, and automatic P&R tools of Avant! co.,Ltd. for layout synthesis. Used process is 0.5 μm CMOS w-metal standard cell array technology provided by NEL(NTT Electronics Technology co.,Ltd.).

Since the gated clock scheme is adopted to vary active data-path width and to invalidate a clock of inactive modules, we use 65 logic gates for clock control. Chip specification is shown in TABLE I.

<table>
<thead>
<tr>
<th>Process</th>
<th>0.5 μm CMOS w-metal</th>
</tr>
</thead>
<tbody>
<tr>
<td>Chip size</td>
<td>4.76μm × 4.76μm = 22.66mm²</td>
</tr>
<tr>
<td>Number of cells</td>
<td>2907 (23,000 tr.)</td>
</tr>
<tr>
<td>Signal pin</td>
<td>76 pins</td>
</tr>
<tr>
<td>Clock frequency</td>
<td>25 MHz</td>
</tr>
</tbody>
</table>

We verified designed chip and estimated power consumption by the post-layout simulation. Estimated power consumption is shown in TABLE II.

- **32-bit mode** All instruction is executed in 32-bit data-path width.
- **8-bit mode** Instructions whose precision is shorter than 8-bit is executed in 8-bit data-path width.

<table>
<thead>
<tr>
<th>Voltage</th>
<th>Datapath Width</th>
<th>Power Consumption</th>
</tr>
</thead>
<tbody>
<tr>
<td>3.3[V]</td>
<td>32 bit mode</td>
<td>321mW @ 25MHz</td>
</tr>
<tr>
<td>2.0[V]</td>
<td>8 bit mode</td>
<td>196mW @ 25MHz</td>
</tr>
</tbody>
</table>

Power consumption in 8-bit mode is less than that in 32-bit mode by 39%. Since power consumption of data-path part account for only 50% of total power consumption, power of 8-bit mode can not be quarter of 32-bit mode. When clock frequency is slowed down to 15MHz, the processor can run correctly in 2.0[V], and power consumption is less than quarter of power consumption in 3.3[V].

![Fig. 3. A microscopic photograph of Power-Pro](image)

### REFERENCES


