Partial Scan Design Methods Based on Internally Balanced Structure

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Abstract—In this paper, we theoretically and experimentally show the effectiveness of partial scan design based on internally balanced structure, which is a sequential circuit capable of generating tests with a combinational test generation algorithm. Moreover, we introduce a method of extended partial scan design, which replaces part of not only flip-flops but also wires by bypass flip-flops in a sequential circuit, and propose a method of extended partial scan design such that the kernel circuit is an internally balanced structure. We present an algorithm for finding a set of flip-flops and wires in order to minimize the area overhead for the extended partial scan design. We consider the test procedure for the kernel circuit using the scan path and the additional circuit by scan design with the partial scan design and the extended partial scan design based on internally balanced structure and demonstrate the effectiveness of the test procedures. Experimental results for ISCAS'89 benchmark circuits show that the proposed partial scan design and extended partial scan design can be implemented with low area overhead.

I. INTRODUCTION

Test generation for a sequential circuit is generally difficult and intractable problem when the scale of the circuit is larger. To solve this problem, full scan design technique, which replaces all the flip-flops by scanable flip-flops (scan flip-flops) in a sequential circuit, have been proposed [1][2]. In full scan design, the circuit which excludes scan flip-flops (kernel circuit) is a combinational circuit so that it is capable of generating tests with a combinational test generation algorithm (capable of combinational test generation) and achieves almost complete fault sensitivity. However, the full scan design technique leads to an overhead in circuit area. Partial scan design, which replaces part of flip-flops by scan flip-flops in a sequential circuit, is one of techniques which implement an easily testable circuit with low area overhead. Partial scan design techniques which require sequential test generation [3][4] for the sequential kernel circuit, however, are still difficult to achieve high fault efficiency. On the other hand, partial scan design such that the kernel circuit is a balanced structure, which is a sequential circuit capable of combinational test generation, has been proposed [5]. We have proposed a sequential circuit with internally balanced structure, which is a circuit extending balanced structure as a sequential circuit capable of combinational test generation, and its application to partial scan design [6].

In this paper, to reduce further area overhead, we introduce a method of extended partial scan design, which replaces part of not only flip-flops by scan flip-flops but also wires by bypass flip-flops[2][7][8] in a sequential circuit, and propose a method of extended partial scan design such that the kernel circuit is an internally balanced structure. We present an algorithm for finding a set of flip-flops and wires in order to minimize the area overhead for the extended partial scan design. We consider the test procedure for the kernel circuit using the scan path and the additional circuit by scan design with the partial scan design and the extended partial scan design based on internally balanced structure and demonstrate the effectiveness of the test procedures. Experimental results for ISCAS'89 benchmark circuits show that the proposed partial scan design and extended partial scan design can be implemented with low area overhead.

II. SEQUENTIAL CIRCUITS CAPABLE OF COMBINATIONAL TEST GENERATION

When a sequential circuit has some feedback loops, it is not capable of combinational test generation [3]. In this section, we restrict the target circuit to a sequential circuit with acyclic structure (with no feedback loops). We restrict flip-flops (FF’s for short) to DFF’s without loss of generality. In the next section, we consider general sequential circuits with feedback loops.

On a fanout point in a circuit, the wire corresponding to an input of the fanout point is called the fanout stem, and the wires corresponding to outputs of the fanout point are called the fanout branches. The sequential depth of a path is the number of flip-flops along the path. The sequential depth of a sequential circuit is the maximum sequential depth among the paths from primary inputs to primary outputs in the sequential circuit. Let \( x \) be a primary input and let \( x_i \) and \( x_j \) be its two fanout branches. If there are no paths with the same sequential depth form \( x_i \) and \( x_j \) to a primary output \( z_k \) then \( x_i \) and \( x_j \) are said to be separable.

Combinational transformation (C-transformation)[6]: The transformation consisting of the two followings operations for an acyclic sequential circuit \( S \) are called the Combinational transformation (C-transformation), and the combinational circuit after the transformation is expressed as \( C(S) \).

(1) For a primary input having some fanout branches,
let $X$ be a set of fanout branches of the primary input. Find the minimal partition $\pi$ for $X$ which satisfies: If fanout branch $x_i$ and $x_j$ belong to different blocks $X(i)$ and $X(j)$, respectively by partition $\pi$ (i.e., $x_i \in X(i)$, $x_j \in X(j)$; $X(i) \neq X(j)$), $x_i$ and $x_j$ are separable. Create new inputs for every partitioned blocks and separate the original primary inputs. (See Fig. 1.)

(2) Replace each FF in $S$ by a wire. (When the negative output of a FF is used, add an inverter. See Fig. 2.)

**Capability of combinational test generation**:

Let $S$ be an acyclic sequential circuit and let $C(S)$ be the CTI-transformed combinational circuit. The sequential circuit $S$ is said to be capable of combinational test generation when it is testable in $S$ if and only if the corresponding fault $f_c$ in $C(S)$ is testable in $C(S)$.

Sequential circuits capable of combinational test generation are the following:

- **Balanced structure**: If all paths for any input-output pairs in a sequential circuit $S$ have the same sequential depth then $S$ is said to be a balanced structure. (See Fig. 3.)

- **Internally balanced structure**: If the circuit $S'$ transformed from $S$ by using only the rule (1) of C-transformation is a balanced structure, then $S$ is said to be an internally balanced structure. (See Fig. 4.)

Since balanced sequential circuits have no separable primary inputs, only the rule (2) of C-transformation is carried out. From the above definition, it is clear that internally balanced structures belong to a larger class of sequential circuits than balanced structures.

### III. Internally Balanced Partial Scan Design

Next we consider a general sequential circuit with feedback loops. Partial scan design such that the rest circuit excluding scan FF’s (the kernel circuit) is an internally balanced structure is called *internally balanced partial scan design*. Internally balanced partial scan design enables test generation using only a combinational test generation algorithm. This issue is discussed further in Section VII. In Section VIII, experimental results for benchmark circuits show that internally balanced partial scan design can be implemented with low area overhead.

### IV. Extended Partial Scan Design

We define *removing* of an element $e$ (FF or wire) in $S$ for a sequential circuit $S$ as replacing the input to $e$ by a primary output of $S$ and the output from $e$ by a primary input of $S$ and separating the element $e$ from $S$. The replaced primary input and primary output are called *pseudo input* and *pseudo output*, respectively. The operation is expressed as operator $-$. For a set of elements $E$ in $S$, $S - E$ defines the circuit removing all elements in $E$ from $S$.

Let $F$ and $L$ be a set of flip-flops and a set of wires in a sequential circuit $S$, respectively. Given a set of the elements $E = \{ FF_1, \ldots, FF_n, l_1, \ldots, l_m \}$ (provided $FF_i \in F$ ($i = 1, \ldots, n$), $l_j \in L$ ($j = 1, \ldots, m$)) in $S$, $S - E$ is called the circuit with respect to $E$, and $FF$’s and wires in $E$ are called external FF’s and external wires, respectively. (See Fig. 5.)

Most partial scan design techniques replace only FF’s by scan FF’s and generate test patterns for the kernel circuit which excludes scan FF’s. However, some partial scan design methods have also been proposed, which replace not only FF’s by scan FF’s but also wires by *bypass FF’s* (which work like scan FF’s)[2][7][8]. As shown in Fig. 6, the partial scan design which replaces external FF’s by scan FF’s and external wires by bypass FF’s is said to be *extended partial scan design*.

For the circuit with extended partial scan design, scan FF’s and bypass FF’s are called *extended scan FF’s* generally.

The structures of each scan FF and bypass FF (S-FF and B-FF for short, respectively) are considered as in Fig. 7 and Fig. 8, respectively. Each S-FF and B-FF have three operation modes: the *normal mode*, the *load mode*, and the *shift mode*, according to the values of the control lines of the multiplexers in each FF as shown in Table I.

In the *normal mode*, each S-FF works as a DFF and each B-FF works as a wire as in Fig. 6 (a). In the load
mode, data are read from the data input of each FF during every clock cycle. In the shift mode, test patterns are scanned in each FF and the value of each FF is scanned out simultaneously through the scan path.

Hold of FF’s means the operation in which they retain their value across consecutive clock cycles. This operation mode is called the hold mode. Each extended scan FF in extended partial scan design is assumed to have the hold mode.

Let \( k_1 \) be the area overhead due to replacing a FF by a S-FF and let \( k_2 \) be the area overhead due to replacing a wire by a B-FF. Then, the total area overhead with extended partial scan design is expressed by the following expression:

The total area overhead

\[
= k_1 \times \frac{\text{number of external FF's}}{\text{number of external wires}} + k_2 \times \frac{\text{number of external wires}}{\text{number of external FF's}}
\]

The ratio of \( k_1 \) to \( k_2 \) is, for example, 3 : 12 provided the hardware amount of a multiplexer and a FF are 3 and 6 gates, respectively, as [9].

Compared to partial scan design scanning only FF’s, extended partial scan design has more freedom to select scan elements and hence low area overhead is expected for its implementation.

V. INTERNALLY BALANCED EXTENDED PARTIAL SCAN DESIGN

For general sequential circuits, extended partial scan design such that the kernel circuit is an internally balanced structure enables test generation using only a combinational test generation algorithm like internally balanced partial scan design. This issue is discussed further in Section VII.

Extended partial scan design such that the kernel circuit is an internally balanced structure is called internally balanced extended partial scan design. In Section VI, we present an algorithm for finding a set of external FF’s and external wires in order to minimize the area overhead for internally balanced extended partial scan design.

VI. EXTENDED SCAN FF’S SELECTION PROBLEM

The problem to find a set of external FF’s and external wires in order to minimize the area overhead when the kernel circuit is an internally balanced structure for a given sequential circuit is called extended scan FF’s selection problem. (See Fig. 9.)

We consider a method to solve the extended scan FF’s selection problem by dividing into the two following steps. However optimal solutions for the individual steps do not imply an optimal overall solution. Dividing the problem has the advantage of being able to transform the problem into the easy one and to use existing algorithms by simple
modification.

1. Acyclic structure

Select a set of external FF’s and external wires to minimize the area overhead such that the kernel circuit is an acyclic structure.

2. Internally balanced structure

For the acyclic kernel circuit obtained by 1.
(2-1) Separate primary inputs whose fanout branches are separable. (except pseudo inputs in the kernel circuit)
(2-2) Select a set of external FF’s and external wires to minimize the area overhead such that the kernel circuit is a balanced structure.

We construct the following graph model for analyzing a sequential circuit to solve the problem.

Definition 1: A circuit topology graph (CTG) for a sequential circuit $S$ is a directed graph $G = (V, A, w)$.

$V$ is the set of nodes representing gates, fanout points, primary inputs and primary outputs in $S$.

$A \subseteq V \times V$ is the set of arcs representing FF’s and wires in $S$ (Each arc represent a connection in $S$).

$w : A \rightarrow Z^+$ (positive integers) defines the weights of the arcs. (FF’s are of weight $k_1$! $\%$ and wires are of weight $k_2$, where $k_1$ is the area overhead due to replacing a FF by a S-FF and $k_2$ is the area overhead due to replacing a wire by a B-FF.)

A CTG $G$ can be transformed into a graph $\bar{G}$ which has less nodes by applying the following transformation rule. As is evident from the transformation rule, the original graph $G$ and the transformed graph $\bar{G}$ have their solutions with the same area overhead for the extended scan FF’s problem.

Transformation rule : Let $G_v$ be an acyclic subgraph of a CTG $G$ which consist of only nodes corresponding to gates and fanout points (except primary inputs and outputs) and weight $k_2$ arcs corresponding to wires. Let $w_i$ be the sum of the weights of the incoming arcs in $G_v$ and let $w_o$ be the sum of the weights of the outgoing arcs in $G_v$. Let $m_v$ be the minimum sum of the weights of the arcs needed to cut all directed paths in $G_v$. If there are paths from each input to all outputs in $G_v$, and

$$m_v \geq \min\{w_i, w_o\}$$

then $G_v$ will be merged into a node $v$ as in Fig. 10. $\square$

Using the above graph model, the procedure to select external FF’s and external wires such that the kernel circuit is an internally balanced structure can be described as follows.

Step 1. Transform the CTG $G$ for a sequential circuit $S$ into an CTG $\bar{G} = (V, A, w)$ by applying the transformation rule.

Step 2. Transform $\bar{G}$ into an acyclic CTG $\bar{G}_A$ by removing a set of arcs $R_A$ such that $\sum_{a \in R_A} w(a)$ is minimized.

Step 3. Transform $G_A$ into a CTG $\bar{G}_A$ by separating primary inputs whose fanout branches are separable.

Step 4. Transform $\bar{G}_A$ into a balanced CTG $G_B$ by removing a set of arcs $R_B$ such that $\sum_{a \in R_B} w(a)$ is minimized.

As a result, $R = R_A \cup R_B$ is the desired set of arcs corresponding to external FF’s and external wires.

At the above Step 2, a set of arcs $R_A$ such that $\sum_{a \in R_A} w(a)$ is minimized is obtained by applying weighted MFAS (Minimum Feedback Arc Set) algorithms.

In this case, assign $k_1$ (FF) or $k_2$ (wire) to each arc weight.

The operation to separate primary inputs at the Step 3 corresponds to the C-transformation (1). At the Step 4, a set of arcs $R_B$ such that $\sum_{a \in R_B} w(a)$ is minimized is obtained by the procedure modifying the balancing procedure in [5]. The balancing procedure in [5] assigns the bit width of the corresponding register to each arc weight. This procedure is applicable to the above balancing problem by replacing each arc weight by $k_1$ (FF) or $k_2$ (wire).

**VII. Test Procedure for Circuit with Partial Scan Design**

The test procedure for the circuit with internally balanced partial scan design and internally balanced extended partial scan design consists of testing the kernel circuit using the scan path and testing the additional circuit by scan design. In this section, we consider the test procedure and show its effectiveness for the circuit with internally balanced partial scan design and internally balanced extended partial scan design. Although the below issue is discussed about the circuit with internally balanced extended partial scan design, it is applicable to the
circuit with internally balanced partial scan design if one consider the case there are no B-FF’s.

Let $S$ be a sequential circuit. Let $S_{DFT}$ be the circuit with internally balanced extended partial scan design for $S$. Let $S_K$ be the circuit removing extended scan FF’s for $S_{DFT}$ (the kernel circuit with internally balanced structure). Let $C(S_K)$ be the C-transformed circuit for $S_K$.

In order to test the circuit with extended partial scan design like $S_{DFT}$ for a sequential circuit $S$, it is required to test all detectable faults in $S_{DFT}$. Faults in $S_{DFT}$ corresponding to $S_K$ are called internal faults in $S_{DFT}$. Faults in $S_{DFT}$ but not in $S_K$ (faults of extended scan FF’s in $S_{DFT}$) are called external faults in $S_{DFT}$. Testing for each type of faults is described as follows.

A. Testing for Internal Faults

Let $f_{DFT}$ be an internal fault in $S_{DFT}$, let $f_K$ be the corresponding fault in $S_K$ and let $f_C$ be the corresponding fault in $C(S_K)$. $f_{DFT}$ is $S_K$, and $f_C$ are one-to-one correspondence each other.

For the circuit $S_{DFT}$ with extended partial scan design such that the kernel circuit $S_K$ is an internally balanced structure, the test sequence for an internal fault $f_{DFT}$ in $S_{DFT}$ is obtained as follows:
1. Generate the test pattern $T_C$ for the fault $f_C$ in $C(S_K)$ corresponding to $f_{DFT}$ by using a combinational test generation algorithm.
2. Transform the generated test pattern into the test sequence $T_K$ in $S_K$.
3. Transform the test sequence in $S_K$ into the test sequence $T_{DFT}$ in $S_{DFT}$.

The detail of the above procedure from 1 to 3 is omitted here due to limitations of space. For further details, refer to [10]. On this procedure, the test generation problem for $f_{DFT}$ in $S_{DFT}$ results in the one for $f_C$ in $C(S_K)$. In order to guarantee test generation using this, it is required to show that a fault $f_{DFT}$ in $S_{DFT}$ is testable in $S_{DFT}$ if and only if the corresponding fault $f_C$ in $C(S_K)$ is testable in $C(S_K)$. This is shown by the following theorem.

From [6], if a sequential circuit $S_K$ is an internally balanced structure then $S_K$ is capable of combinational test generation, therefore, this leads to the next theorem.

**Theorem 1**: Let $S_K$ be a sequential circuit with internally balanced structure. A fault $f_K$ in $S_K$ is testable in $S_K$ if and only if the corresponding fault $f_C$ in $C(S_K)$ is testable in $C(S_K)$.

The above procedure for test sequences from 1 to 3 [10] and Theorem 1 lead to the next theorem.

**Theorem 2**: Let $S_K$ be a sequential circuit with internally balanced structure. If a fault $f_K$ in $S_K$ is redundant, the fault $f_C$ in $C(S_K)$ corresponding to $f_K$ is decided to be redundant by procedure 1. If a fault $f_K$ in $S_K$ is testable, the test sequence $T_K$ and $T_{DFT}$ obtained by procedure 2 and 3 are the test sequences for the corresponding faults $f_K$ in $S_K$ and $f_{DFT}$ in $S_{DFT}$, respectively.

In order to explain that Theorem 2 is valid for internal faults in $S_{DFT}$, it is required to show the next theorem.

**Theorem 3**: Let $S_K$ be a sequential circuit with internally balanced structure and let each extended scan FF in $S_{DFT}$ have the hold mode. Then a fault $f_K$ in $S_K$ is testable in $S_K$ if and only if the corresponding fault $f_{DFT}$ (an internal fault) in $S_{DFT}$ is testable in $S_{DFT}$.

(Proof) The proof of the necessary condition is evident from the above procedure transform the test sequence into $S_{DFT}$ by partitioning $S_{DFT}$ into the kernel circuit and the remaining circuit, and explaining that testing for a fault $f_{DFT}$ in the kernel circuit of $S_{DFT}$ is one for the corresponding fault $f_K$ in $S_K$. For further details, refer to [11].

B. Testing for External Faults

For external faults (faults of extended scan FF’s) in $S_{DFT}$, the following theorem holds.

**Theorem 4**: Let $S_{DFT}$ be a circuit with extended partial scan design such that the kernel circuit is an internally balanced structure. Then all irredundant faults of S-FF and B-FF in $S_{DFT}$ are testable.

The proof of the theorem and the details of the test sequences are omitted here due to limitations of space. For further details, refer to [11].

VIII. Experimental Results

Using the techniques in Section VI, the experiment finding external FF’s and external wires such that the kernel circuit is an internally balanced structure is carried out for ISCAS’89 benchmark circuits. Let $k_1$ be the hardware overhead due to replacing a FF by a S-FF and let $k_2$ be the hardware overhead due to replacing a wire by a B-FF. Here we assumed $k_1 : k_2 = 1 : 4$. The experimental results are shown in Table II. In Table II, GGB refers to the area overhead (the number of scan FF’s) for the partial scan design such that the kernel circuit is a balanced structure [5]. Method 1 refers to the area overhead (the same) for internally balanced partial scan design. Method 2 refers to the area overhead (where FFs and Wires refers to the number of external FF’s and external wires, respectively) for internally balanced extended partial scan design. From the result in Table II, s15850, s15850.1 and s35932 show that Method 1 can be implemented with low area overhead compared to GGB [5] by the effect of separating primary inputs. Moreover, s13207, s13207.1 and s38417 show that Method 2 can be implemented with the least area overhead among three methods by the effect selecting wires. However the other circuits have the same results as GGB. On the whole, Method 1 has better results than GGB and Method 2 has better results than Method 1.
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IX. CONCLUSIONS

We have considered internally balanced structure as a sequential circuit capable of combinational test generation. We have presented a method of partial scan design and extended partial scan design such that the kernel circuit is an internally balanced structure and explained their properties. Compared to partial scan design scanning only FF’s, extended partial scan design has more freedom to select scan elements by selecting wires and hence low area overhead is expected for its implementation. We have considered an algorithm for finding a set of external FF’s and external wires in order to minimize the area overhead for extended partial scan such that the kernel circuit is an internally balanced structure. Moreover, for the circuit with partial scan design and extended partial scan design such that the kernel circuit is an internally balanced structure, we have presented the test procedures using the scan path and showed that those test sequences can be transformed from test patterns generated by a combinational test generation algorithm. Finally, experimental results for ISCAS’89 benchmark circuits have shown that the proposed partial scan design and extended partial scan design can be implemented with low area overhead.

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