TCAD/DA for MPU and ASIC Development

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Abstract--- We have proposed, in this paper, a, TCAD/DA methodology for MPU and ASIC with updated processes and devices, which allow a predictive chip-design with quick quantitative correlation studies between process-recipe and CKT & delay parameters required in DA works. Effects of statistical process variation on 0.35um CMOS have been rigorously characterized with a new global TCAD calibration technique. Based on the data, process variation effects on a 0.25um CMOS have been predicted, which is concluded that the Vth and Ids total-variation of the 0.25um CMOS shows less than 10% in production process, which is similar with that of the 0.35um CMOS.

I. INTRODUCTION

In quarter-um CMOS, statistical process variation control becomes one of the crucial issues to achieve high-performance CMOS MPU and ASIC. Device performances vary in various process step sequence, also gate-delay distribution affects clock-timing margin. Therefore, circuit and chip designer needs a quick evaluation and validation of process and devices in terms of worst-case and/or statistical performance design before actual mass-production phase. In chip design, increasing requirement on high-speed operation (clocking) forces a precise clock-distribution design as well as accurate gate & interconnect delay estimation, with minimal design margin taken into account the process variation effects.

In such a situation, great interests has been arisen on the TCAD to reduce design TAT (turn-around time) of VLSIs, since process & device scaling is thought to be one of the practical chip-performance improvement techniques and the chip-performance and its statistical variation are tightly coupled with the shrunken process especially in sub-half um CMOS. We have proposed, in this paper a, TCAD/DA methodology for MPU and ASIC with updated processes and devices, which allow a predictive chip-design with quick quantitative correlation studies between process-recipe and CKT & delay parameters required in DA works.

II. TCAD/DA FOR PROCESS & CHIP CONCURRENT DESIGN

In quarter-um CMOS, concurrent design of process and chip is extremely important in Giga-Flops MPU and high-performance ASIC. To achieve the concurrence, quick and predictive diagnosis between the updated process and CKT performances have been done since the chip-performance and its statistical variation are tightly coupled with the shrink process in sub-half um CMOS, as mentioned before. Conventional method of experimental Test- Structure fabrication and CKT parameter extraction do not allowed because of the increasing cost (8-inch wafer) and technological difficulties in newly utilized (or expected) process equipment. In this context, the TCAD application accompanied with reasonable calibration techniques looks very promising to answer the demand of concurrent design of process and chip.

Fig. 1 shows a proposed TCAD/DA methodology, aiming the concurrent process and MPU & ASIC development. Because of the importance of delay and high-speed clock design in updated MPU and ASIC, a delay-specification and design has been newly introduced in chip development hierarchy as shown in the figure. The key role of TCAD is QTAT as well as predictive generation of gate/interconnect delay parameter library for the upcoming DA works, in such a way that it reflects the effects of continuously updating CMOS process recipes, on chip performance of speed, power and reliabilities.

Details of the TCAD is divided to a couple of sub-topics; (1) predictive process and device characterization, (2) CKT model parameter generation, (3) diagnosis of statistical process variation effect[1], (4) delay modeling and interconnect characterization, and (5) parametric yield enhancement in a new chip production, as shown in Fig. 1. Some of the above are still infant phase, however, a good many TCAD activities have been performed as described below.

III. TCAD FOR A 0.25UM CMOS ASIC

In this paper, effects of statistical process variation on 0.35um CMOS have been rigorously characterized. To achieve ANOVA (analysis of variance), a series of TCAD and the RSM (Response Surface Method)[2] on the CMOS process and devices have been efficiently utilized with a new global calibration technique. It gives excellent experimental accuracy of the generated model within
0.02V error in the threshold voltage (Vth) and 3% error in the drain maximum current (Ids). Each process recipe is diagnosed statistically its variation effects on the devices for the first time. Furthermore, process variation effects on a 0.25um CMOS have been predicted based on the TCAD-ANOVA. It is concluded that the Vth and Ids total-variation of the 0.25um CMOS shows less than 10% δIds in production process, which is similar with that of the 0.35um CMOS.

Additional TCAD generated MOS model & capacitive parameters, which allows circuit-designers to use them in predictive worst-case design before chip fabrications. Preliminary study on 0.25um NMOS fabrications verify its reasonable accuracy of the predicted Ids variation within 5% errors.

Process variation effects on device characteristics are evaluated using 0.35um CMOS experimental results, in production level, and TCAD-based metrology. Experimental Ids (normalized) distributions of 0.35um NMOS is shown in Fig. 2. The 345 Ids-data were collected from a couple of months electric-test data. In the figure, the Ids variations (3σ) for both design specification and real experimental data are demonstrated, which make it clear that the original specification of δIds does not reflect correctly the actual production level process variation (over specification). It is noted that the over specification of process variation results in difficulties in worst case design for optimum high speed clock distribution network. To achieve rigorous component analysis of the process variation on the Ids distribution, we have developed a new TCAD-based metrology. Physical models and their parameters are firstly verified with in-house TED (Transient Enhanced-Diffusion) database built with more than 300 SIMS data[3]. With the TCAD database, the 0.35um device’s Vth and Ids were simulated and verified with corresponding experiments as shown in Fig. 3. It shows that the both results coincide each other, including reverse-short-channel (RSC) effect on Vth-Lg curves. However, this result is relatively lucky case. In many cases, significant discrepancy between TCAD and experiments can be seen, even if we calibrate impurity profile with our TED-database.

Response Surface Function (RSF) is employed to achieve quantitative process sensitivity analysis on the Ids and Vth. In Table 1, we show an example of a variable transformation for five-process recipe, which demonstrate a new transformation of Lg being used to reflect RSC effect. Experimental global calibration[2] is conducted, after obtaining TCAD-based RSF for Vth and Ids as parameters of Lg, Tox and channel doping conditions. A novel extraction procedure in the RSF calibration has been devised to realize physically sounds RSFs, which avoids non-physical artificial fitting to the experimental data. It is noted this step is important to get reliable RSF which can be used in practical process/device ANOVA. Fig. 4 shows resulting calibrated RSFs on the Vth and Ids, which clarify an excellent agreement within errors of 0.02V for the Vth and 3% for the Ids including worst-case doping conditions. Fig. 5 shows predicted process sensitivity analysis on the Ids variation by assuming process parameter fluctuations of +/- 10%. Note the Tox fluctuation affects much in the Ids variation more than the Lg variation effect in the 0.35um NMOS. In Fig. 6, Vth and Ids distributions are compared between the experiments (>1000 samples) and RSF Monte-Carlo, which proves validity of the proposed TCAD-ANOVA.

To predict 0.25um CMOS process sensitivity, we investigated actual process variations of Lg CD (Critical Dimension) control, Tox variation and implant dose etc. The measured Lg variation using 705 points POC (Process Quality Control)data (> 100 wafers) is shown in Fig. 7, as an example. Based on these data, a rigorous process component analysis on the δIds are conducted and shown in Table 2 for 0.35um and a newly optimized 0.25um CMOS process/device, which is derived with the calibrated RSF. Experimental comparison clarifies that experimental δIds agree well with the one calculated in 0.35um CMOS RSFs. Also the predicted 0.25um process shows a good process controllability as that of 0.35um process for both N and PMOS. Note that correlation of each recipe is found to be quite small on the total δIds in these CMOS processes, which means process conditions listed in the recipe of Table 2 shows closely independent each other, in terms of the δId due to process variation.

Worst-case process conditions has been determined based on circuit types and chip performance estimation methodology. Additional TCAD generate the I-V curves for the worst-cases, and parameter extraction has been conducted for a compact MOS model. Examples of the generated a Compact MOS Model parameters for the typical and worst-cases are shown in Fig. 8, in the forms of Ids-Lg and Vth-Lg curves. To predict gate-delay and interconnect delay, worst case capacitance and wire resistance are required. Worst-case parameters for interconnects capacitance has been determined with the design-chart[4], which is formed with extensive 3D device simulations. TCAD generated junction capacitance (Cj) process sensitivity data is also used in estimating worst case capacitive load of circuits. as shown in Fig. 9. By adding statistical PQC-data of inter layer wiring resistance, a delay parameter library for a 0.25um CMOS ASIC can be constructed after months of circuit simulation work.

IV. Conclusion

We have proposed, in this paper a TCAD/DA methodology for MPU and ASIC with updated processes and devises, which allow a predictive chip-
design with quick quantitative correlation studies between process-recipe and CKT & delay parameters required in DA works. Effects of statistical process variation on 0.35um CMOS have been rigorously characterized. A series of TCAD and the RSM on the CMOS process and devices have been utilized with a new global calibration technique. It gives experimental accuracy of the generated model within 0.02V error in the Vth and 3% error in the Ids. Each process recipe is diagnosed statistically its variation effects on the devices for the first time. Furthermore, process variation effects on a 0.25um CMOS have been predicted based on the TCAD. It is concluded that the Vth and Ids total-variation of the 0.25um CMOS shows less than 10% Ids in production process, which is similar with that of the 0.35um CMOS. Additional TCAD generated MOS model & capacitive parameters, which allows circuit-designers to use them in predictive worst-case design before chip fabrications. Preliminary study on 0.25um NMOS fabrications verify its reasonable accuracy of the predicted Ids variation within 5% errors.

REFERENCES


Fig. 1 CAD/DA for MPU and ASIC Chip Developmer
Normalized I

Fig. 2 Comparison of specification and a

Fig. 3 TCAD simulation with T and experiments of

Fig. 4 Globally calibrated RSF achieved with TCAD and new coefficients extraction excellent agreement with experimental data of Vth & Ids-Lg curves.
Fig. 5 Predicted process sensitivity on the 0.35um NMOS I:

Table 1 RSF variable transform reflects RSC-eff

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Function</th>
<th>Center</th>
</tr>
</thead>
<tbody>
<tr>
<td>Implant</td>
<td>$Y(x_0)$</td>
<td>$x_0$</td>
</tr>
<tr>
<td>Implant</td>
<td>$Y(x_0)$</td>
<td>$x_0$</td>
</tr>
<tr>
<td>Implant</td>
<td>$Y(x_0)$</td>
<td>$x_0$</td>
</tr>
<tr>
<td>Lg</td>
<td>$Y(x_0)$</td>
<td>$x_0$</td>
</tr>
<tr>
<td>Tox</td>
<td>$Y(x_0)$</td>
<td>$x_0$</td>
</tr>
</tbody>
</table>

Fig. 6 Vth and Ids distributions compared between experiment and RSF Monte-Carlo.
Fig. 7: Actual process variations of Lg

![Graph showing counts against Lg (normalized) ranges including -0.1 to 0.1.]

The number of total Lg data

Counts

Lg (normalized)

Fig. 8: Generated worst-case MOS model parameters determined based on the TCAD-ANOVA for 0.25um CMOS.

![Graph showing Ids (mA) against Lg (µm) with typical, +10%, and -10% conditions.

Typical

Tox +10%

Tox -10%

Fig. 9: Cj variation component-analysis for implanted-dose condition

Table 2: Process component sensitivity analysis on the device performance

<table>
<thead>
<tr>
<th>Ids</th>
<th>NMOS</th>
<th>PMOS</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>0.3µm</td>
<td>0.2µm</td>
</tr>
<tr>
<td>Process Parameter</td>
<td>CMOS</td>
<td>CMOS</td>
</tr>
<tr>
<td>Lg</td>
<td>13.4%</td>
<td>16.7%</td>
</tr>
<tr>
<td>Implant 1</td>
<td>10.6%</td>
<td>10.7%</td>
</tr>
<tr>
<td>Implant 2</td>
<td>11.5%</td>
<td>10.2%</td>
</tr>
<tr>
<td>Implant 3</td>
<td>11.0%</td>
<td>10.5%</td>
</tr>
<tr>
<td>Tox</td>
<td>16.4%</td>
<td>16.7%</td>
</tr>
<tr>
<td>Wg</td>
<td>14.0%</td>
<td>10.3%</td>
</tr>
<tr>
<td>Total Sensitivity</td>
<td>18.3%</td>
<td>19.5%</td>
</tr>
</tbody>
</table>

Total Sensitivity (Experiment): 18.1% (0.3µm CMOS), 19.5% (0.2µm CMOS).