High-speed GaAs MESFET Digital IC Design for Optical Communication Systems

Kimikazu Sano, Koichi Narahara, Koichi Murata, Taiichi Otsuji, *Kiyomitsu Onodera

NTT Optical Network Systems Laboratories, * NTT System Electronics Laboratories

3-1 Morinosato Wakamiya, Atsugi, Kanagawa, 243-01, Japan

Tel: +81 462 40 2638

Fax: +81 462 40 4146

e-mail: {ksano, murata, narahara, otsuji, onodera}@aecl.ntt.co.jp

Abstract - This paper describes a high-speed GaAs MESFET digital IC design for optical communication systems. We propose novel circuit configurations of a selector and a static delayed flip-flop which are key elements to perform high-speed digital functions. Employing these new design, the selector IC and static decision IC fabricated with 0.12-μm GaAs MESFET operated up to 44 Gbit/s and 22 Gbit/s, respectively. These performances are record speed for GaAs MESFETs.

I. INTRODUCTION

10-Gbit/s commercial transmission systems are installed in backbone networks[1]. However, because of the rapid growth of multimedia services, larger transmission capacities are required for optical communication systems. High-speed electronic components are important for developing cost-effective systems. The next generation of systems requires 20-40 Gbit/s class ICs.

In terms of device speed, InP based heterostructure transistor (HEMT) has the highest potential in developing 20-40 Gbit/s class ICs. A 40-Gbit/s HEMT IC chip set used for the optical communication has already been demonstrated[2]. In terms of device maturity and process simplicity, however, GaAs MESFETs are more attractive, and are likely candidates for 20-40 Gbit/s class ICs.

We have recently reported on a 40-Gbit/s dynamic decision IC fabricated with 0.15-μm GaAs MESFETs which have the average cut-off frequency, f_T, of around 100 GHz[3]. We adopted new circuit configurations such as the super-dynamic Delayed Flip-Flop (D-FF)[4] and wide-band data and clock buffers which employ an inductor peaking and a capacitor peaking. This is because the device speed is not affordable for IC operation and increasing the device speed by shrinking the device feature size is too difficult. Using these high-speed digital and analog circuit techniques, the operation speed of the decision IC reached 40% of f_T. In order to develop 20-40 Gbit/s class GaAs MESFET ICs with a high operating margin, advances in circuit design are needed not only for the dynamic decision IC but also for other digital ICs such as the selector IC and the static decision IC.

This paper describes new circuit configurations for GaAs MESFET selector IC and static decision IC. The selector IC is used in the multiplexer for the time division multiplexing in transmission systems. The static decision IC covers lower speed operations, which the dynamic decision IC cannot handle, and is a fundamental element to be widely used in the multiplexer and demultiplexer. To evaluate the performance of these new circuits, we fabricated ICs with 0.12-μm GaAs MESFETs with an f_T of 97 GHz. The new circuit configurations resulted in a sufficient speed margin for 40-Gbit/s operation of the selector IC and 20-Gbit/s operation of the static decision IC.

II.CIRCUIT DESIGN

A. Selector IC

Figure 1 shows the fabricated selector IC. It consists of two input data buffers, a clock buffer, a selector core circuit, an output buffer, and an output driver. All of them were designed with the Source-Coupled FET logic (SCFL). In order to obtain a clear eye opening, inputs and outputs were respectively terminated with 50-Ω and 100-Ω resistor. The IC has single-ended data, clock inputs and differential data outputs.

Buffers were improved to cover the frequency range needed for 40-Gbit/s signal amplification. We employed inductor peaking amplifiers in the clock buffer and the output buffer. To compensate for the loss of the gain at high frequencies in source followers, capacitor peaking was also added.

Figure 2 shows the circuit diagram of the new selector core circuit. A parallel feedback circuit[5] was added to the clock input differential gate, and inductors were connected to the load resistors in series. In the selector core, the highest frequency component at the output is equal not to the input data frequency but to the input clock frequency. Therefore, the AC characteristic along with the signal path from the clock input to the output is the most critical for the circuit speed. Figure 3 shows calculated gain-bandwidth characteristics of the clock-to-data path for several types of selector circuits. The gain in the low frequency region is boosted by adding a parallel feedback circuit to clock input gates. The feedback resistance RF was designed so as to maximize the DC gain of the circuit. Also, inductor peaking compensates for the losses of the gain in the high frequency region. Both the gain and bandwidth were improved simultaneously by applying the two analog wideband design techniques to the selector circuit. The new circuit is expected to improve the maximum operating speed by more than 10% faster than that of conventional ones.

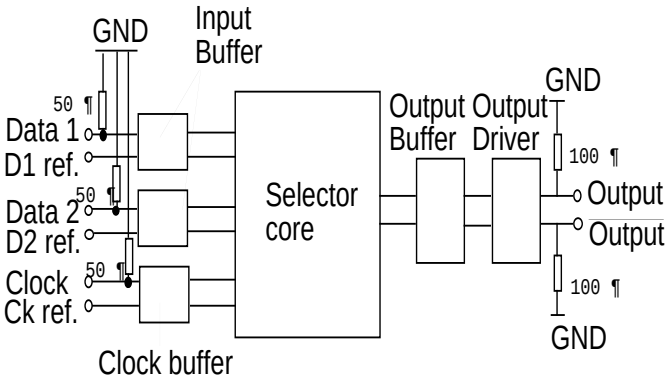

Fig. 1. Block diagram of the fabricated selector IC

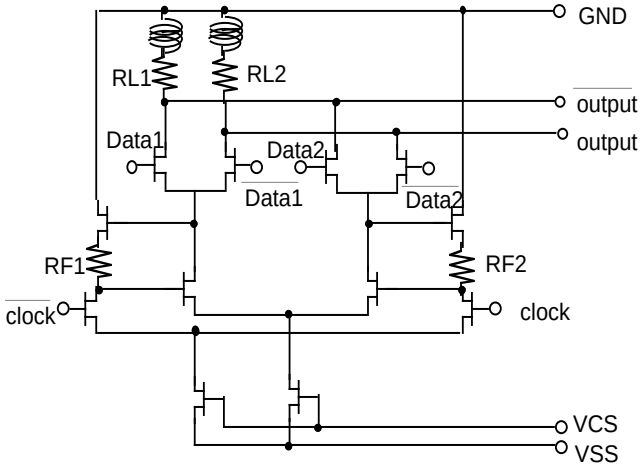

Fig. 2. Novel selector core circuit

B. Static Decision IC

Figure 4 shows the block diagram of the fabricated decision IC. It consists of an input data buffer, a clock buffer, a static D-FF core, an output buffer, and an output driver. Using the same design concept of the selector IC buffers, the static decision IC buffers are designed to cover the frequency range needed for 20-Gbit/s IC operation. The circuitry and the termination resistors are also the same as the selector IC.

In order to obtain a high-speed decision operation, reducing the voltage swing without degrading the slew rate is effective, because it shortens the transition time. To do this, we devised a new static D-FF. Figure 5 shows the circuit diagram of the new D-FF core circuit. In the figure, MR is the data reading source coupled pair (SCP) in the master part and ML is the data latching SCP in the master part, while SR and SL are data reading and latching SCPs in the slave part. The FETs for the clock input are indicated by A and B. We define I1 and I2 as the drain current of FET A through the MR (for I1) and the SL (for I2),

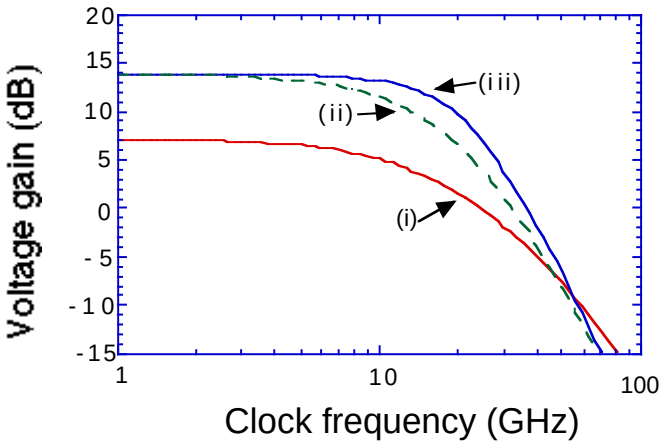

Fig.3. Caluculated gain-bandwidth of selector core.
-(i) Without parallel feedback circuit and inductor.
(ii) Including only parallel feedback circuit.
(iii) Including both parallel feedback circuit and inductor.

when FET A is in the on state and FET B is in the off state and the current from the current source CS passes only through FET A. Similarly, I3 and I4 are defined as the drain current of FET B through the ML (for I3) and the SR (for I4), when FET B is in the on state and FET A is in the off state.

The D-FF has two new features. One is the reduction of the number of circuit elements. The MR and the SL are coupled to create a common source, and the ML and the SR are also coupled. Furthermore, the second level differential pairs are merged into a single pair. This simplified configuration resulted in the drain current of FET A switching to that of FET B when the clock signal is inverted. Thus, we can attain the relationship

$$I1+I2=I3+I4 \quad (1)$$

The second feature is the voltage bias levels fed to each SCP. The bias level of the MR is set higher than that of other SCPs. This is attained by connecting the gate terminal of the MR to the anode of the upper diode of the source follower circuit. As a result,

$$I1>I2 \quad (2)$$

For the ML and the SR, the gate terminals are common and the bias levels are the same,

$$I3=I4. \quad (3)$$

Next, we turn to the principle of operation. From relationships (1), (2) and (3), we can derive

$$I1>I3=I4>I2. \quad (4)$$

Since the logic swing of each SCP is given by the products of load resistance and the currents, the output voltage of the SL is smaller than that of the MR. The transition time between the logical high and low levels is reduced in proportion to the reduction of the effective logic swing, since the signal slew rate is not degraded in this circuit. The combination of the two features in the D-FF reduces the voltage amplitude of data latching and results in higher bit-rate operation. Simulation indicates that the new decision IC can operate over 10% faster than the conventional decision IC.

III. FABRICATION

The selector IC and the static decision IC were fabricated with 0.12-μm n^+-self-aligned Au/WSiN gate GaAs MESFETs[6]. A 0.12-μm gatelength was obtained by using ECR plasma RIE and i-line photolithography with shrinkage of the resist size. We adopted a two-step buried p-layers (BP)

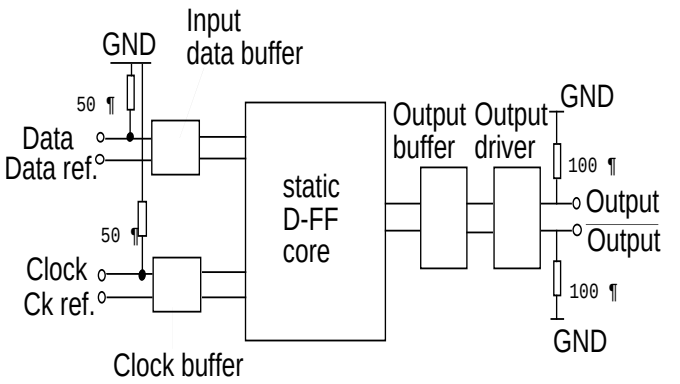

Fig. 4. Block diagram of the fabricated decision IC.

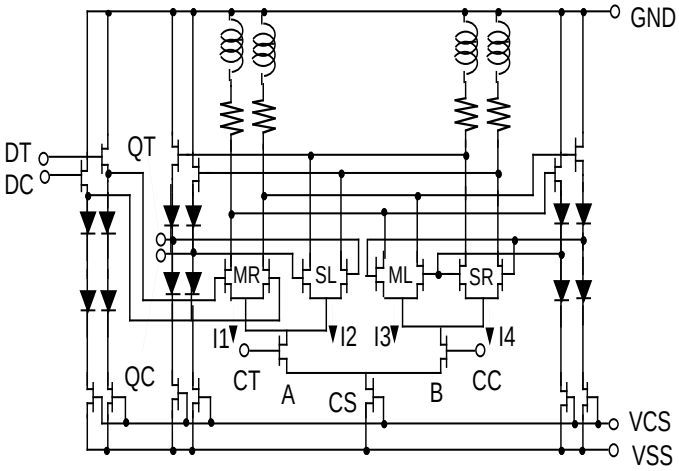

Fig. 5. Novel D-FF core circuit.

LDD structure to suppress the short channel effect. As a result, a low drain-conductance of 31.4 mS/mm was attained while maintaining a high transconductance of 481 mS/mm. The threshold voltage Vth was 0.0V. The average cut-off frequency f_T was 97.5 GHz, and the maximum frequency of oscillation f_{max} was 96.3 GHz. Two conductor levels of Au were employed for the interconnection. The individual conductor levels were separated by a 2.5-μm thickness poliymide. The chip size of both the selector IC and the static IC was 2.0 mm x 2.5 mm.

IV. EXPERIMENTS

A. Selector IC

The IC was tested on a wafer using dedicated 40-GHz bandwidth multicontact RF probes. A complementary pair of 11-Gbit/s pseudorandom bit streams with a length of 2^{23}-1 was duplexed by the GaAs MESFET MUX module in order to obtain 22-Gbit/s data streams. They were then input to the selector IC with an appropriate delay between them. A 22-GHz clock

signal was also input to the selector IC.

Figure 6 shows the output waveforms at 40 Gbit/s and 44 Gbit/s. Good eye openings with 850 mVp-p were obtained at each bit rate. The power dissipation was 0.95 W at a supply voltage of -4.5 V. The 44-Gbit/s operation is the fastest operating speed of the selector IC fabricated with GaAs MESFETs.

For comparison, we also fabricated a conventional selector IC that consists of a conventional selector core and the same input/output buffers as used for the new selector IC. The conventional selector IC operated up to 40 Gbit/s (10% slower than the new one), confirming that the new selector circuit improves circuit speed.

B. Static Decision IC

We obtained a 22-Gbit/s data stream by duplexing a complementary pair of 11-Gbit/s pseudorandom bit streams with a length of 2^{23}-1. Error free operation could be estimated for up to 22 Gbit/s using the 11-Gbit/s Si bipolar decision circuit and the 11-Gbit/s error detector.

Figure 7 shows the input and output waveforms at 20 Gbit/s. A good eye opening with a 750 mVp-p swing was obtained. Error free operation of the decision IC was confirmed from 1 Gbit/s to 22 Gbit/s. The input sensitivity was 180mV and phase margin was 238 degrees at 20 Gbit/s. The power dissipation was 1.08 W at a supply voltage of -4.5 V.

A decision circuit using a conventional master-slave D-FF was also fabricated for comparison. Error free operation of the conventional decision IC was confirmed for up to 20 Gbit/s. The input sensitivity was 669 mV and the phase margin was 122 degrees at 20 Gbit/s.

In terms of the operating speed, the new IC is 10 % faster than the conventional operating speed. Both the input sensitivity and the phase margin around 20 Gbit/s are drastically improved (Figure 8). At 20 Gbit/s, the novel IC has phase margin 194% wider and sensitivity 71% better than the conventional one. Therefore, the novel decision IC is applicable to practical 20-Gbit/s use.

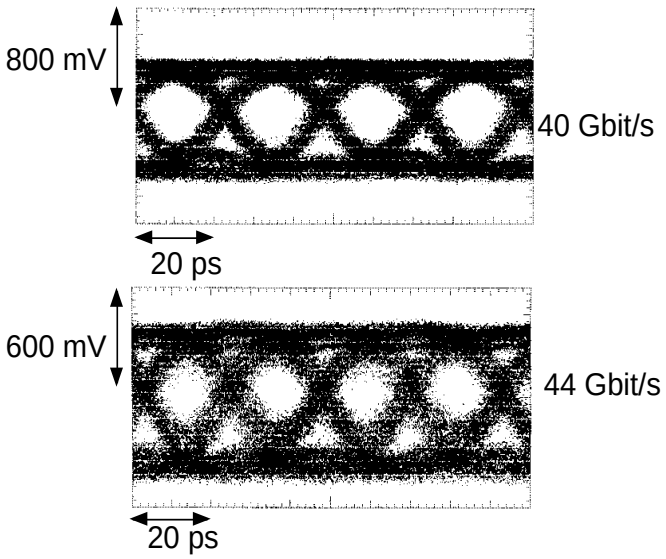

Fig. 6. Waveforms of new selector IC at 40 Gbit/s and 44 Gbit/s.

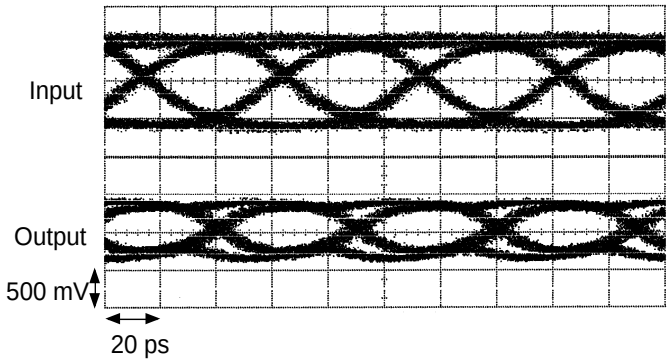

Fig. 7. Waveforms of new decision IC at 20 Gbit/s.

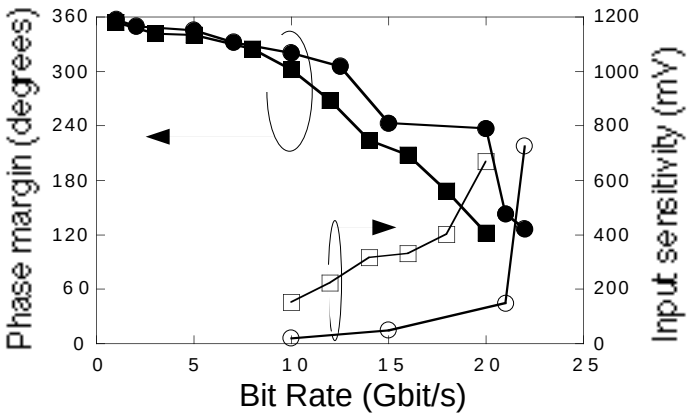

Fig. 8. Input sensitivity and phase margin of decision ICs.
-circles: novel decision IC.
squares: conventional decision IC.

V. CONCLUSION

We have proposed new circuit techniques for the selector IC and the static decision IC for the optical communication systems. The effectiveness of these techniques was confirmed by the fabricated ICs using the 0.1-μm class GaAs MESFET. The novel selector IC operated up to 44 Gbit/s and 10% faster than the conventional IC. The new static decision IC operated up to 22 Gbit/s and attained a bit-rate operation 10% higher than the conventional decision IC. These circuit techniques are important for improving the circuit speed performance while mitigating device requirements.

ACKNOWLEDGEMENTS

The authors would like to thank H. Yoshimura, I. Kobayashi, and K. Yamasaki for their encouragement during this work.

REFERENCES

[1] K. Hagimoto, "Experimental 10 Gbit/s transmission systems and its IC technology, " in GaAs IC Symp. Tech. Dig., pp. 7-10, 1993.

[2] M. Yoneyama, A. Sano, K. Hagimoto, T. Otsuji, K. Murata, Y. Imai, S. Yamaguchi, T Enoki, and E. Sano, "Optical Repeater Circuits using 40-Gbit/s InAlAs/InGaAs HEMT Digital IC Chip Set," in 1997 IEEE MTT-s IMS Tech. Dig., pp. 461-464, 1997.

[3] K. Murata, T. Otsuji, M. Yoneyama, M. Tokumitsu, "A 40 Gbit/s super-dynamic decision IC using 0.15-μm GaAs MESFETs," in 1997 IEEE MTT-s IMS Tech. Dig., pp. 465-468, 1997.

[4] T. Otsuji, M. Yoneyama, K. Murata, and E. Sano, "A Super-Dynamic Flip-Flop Circuit For Broadband Application up to 24-Gbit/s Utilizing Production-Level 0.2-μm GaAs MESFETs," in GaAs IC Symp. Tech. Dig., pp. 145-148, 1996.

[5] N. Ishihara, S. Konaka, T. Kamoto "3.5 GHz bandwidth, 30dB gain Si monolithic amplifier," IEE Electron. Lett. Vol. 25, No. 3, pp. 217-218, 1989.

[6] M. Tokumitsu, M. Hirano, T. Otsuji, S. Yamaguchi, and K. Yamasaki, "A 0.1-μm Self-Aligned-Gate GaAs MESFET with Multilayer Interconnection Structure for Ultra-High-Speed ICs," in IEDM Tech. Dig. pp. 211-214, 1996.