SLICIBILITY OF RECTANGULAR GRAPHS AND FLOORPLAN OPTIMIZATION

Partha S. Dasgupta
MIS Group
IIM Calcutta, Calcutta 700 027
partha@iimcal.ernet.in

Susmita Sur-Kolay
Department of CSE
Jadavpur University, Calcutta 700032
elcv9602@isical.ernet.in

ABSTRACT

The graph dualization approach to floorplan design with rectangular modules usually involves topology generation followed by sizing. The sizing problem for nonslicible topologies is NP-complete. Slicible topologies are often preferred for their simplicity and efficiency. Linear time algorithms exist for generation of topology corresponding to a given rectangular graph, but these do not guarantee slicible topologies even if one exists. Moreover, there is a class of rectangular graphs, known as inherently nonslicible graphs, which do not have any slicible topologies. Previous methods for efficient generation of a slicible topology under sizing constraints for any rectangular graph, are likely to require addition of pseudo-blocks, thereby more empty area. In this paper, new tighter sufficiency conditions for slicibility of rectangular graphs are postulated and utilized in the generation of slicible area-optimal floorplans. These graph-theoretic conditions not only capture a larger class of slicible rectangular graphs but also help in reducing the total effort for unified topology generation and sizing.

Keywords: Very large scale integration (VLSI), Floorplanning, Slicible Floorplans, Nonslicible Floorplans, Heuristic Search, Planar Graphs, Graph Dualization.

1. INTRODUCTION

Floorplanning is an important phase of VLSI physical design cycle. It determines the topology of the layout, i.e., the relative positions of the logical modules on the chip, based on the interconnection requirements of the circuit, the dimensions of the logical modules and estimates for area, wire length, etc. The floorplan optimization problem consists of finding a suitable topology and sizing[5]. A well-known approach to floorplan topology generation is based on graph dualization [4]. The interconnection requirements among the different functional modules in a floorplan are generally represented by an adjacency graph. A floorplan and its adjacency graph have a geometric duality relation. Characterization of adjacency graphs which have a rectangular floorplan realization is given in [4]; such graphs are called rectangular graphs.

In the floorplan optimization problem, various objective

Permission to make digital/hard copies of all or part of this material for personal or classroom use is granted without fee provided that the copies are not made or distributed for profit or commercial advantage, the copyright notice, the title of the publication and its date appear, and notice is given that copyright is by permission of the ACM, Inc. To copy otherwise, to republish, to post on servers or to redistribute to lists, requires specific permission and/or fee

ISPD' 97 Napa Valley, California USA Copyright 1997 ACM 0-89791-927-0/97/04 ..\$3,50

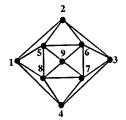


Fig. 1: An INS Graph

functions such as the area and the perimeter of the outermost bounding rectangle, the total wire length for interconnecting the modules, or some other routing area estimate are commonly used. In many cases, a good estimate of the areas of the building blocks are available at this stage, although their aspect ratios may vary over a wide range. Area-optimal floorplan generation based on graph dualization, appear in [1, 3, 4, 10]. It was established in [6] that there is a class of rectangular graphs, called Inherently Nonslicible (INS) (Fig. 1), which do not have any slicible floorplan realization. Although certain sufficiency conditions for slicibility have been formulated [7, 9], exact characterization of INS graphs is still unknown. Hence, given an input rectangular graph, none of the existing polynomial time algorithms can guarantee a slicible floorplan for it, even if one exists. Since slicible floorplans are often preferred due to their simplicity in sizing [5, 8] with respect to the nonslicible ones, our emphasis here is on the generation of area-optimal slicible floorplans without using pseudo-blocks, for a larger subset of non-INS graphs.

The paper is organized as follows: main results are summarized in Section 2, preliminaries appear in Section 3, then the key theorem on tighter sufficiency conditions for slicibility is established in Section 4. The unified floorplanning algorithm using the new criteria is outlined in Section 4 and concluding remarks are presented in Section 5.

2. MAIN RESULTS

In graph dualization, a major condition for rectangular floorplan realization is that the graph must not contain any complex triangle. In [9], it has been shown that with an additional constraint that the input graph contains no complex cycle of length 4 (complex 4-cycles), slicible floorplans always exist. In this paper, a stronger condition for slicibility is proved. It is also shown that even if a rectangular graph contains complex 4-cycles, it is necessarily slicible, provided either all complex 4-cycles in the graph are maximal, or there does not exist any complex 4-cycle in the graph whose all four vertices are assigned to be corners of the corresponding floorplan.

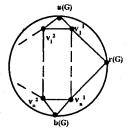


Fig. 2: BFS ordering of extended rectangular graph

Based on these conditions, the unified floorplan optimization method of [2, 3] is adapted to generate slicible floorplans for a larger set of input rectangular graphs, and nonslicible ones for the rest. For an input graph, first all the complex 4-cycles are detected and if these are maximal, i.e., not contained in any other complex 4-cycle, an area-optimal slicible floorplan is produced. The subgraph contained within a maximal complex 4-cycle is replaced by a super-vertex. The method suggested in [3] is then recursively applied to the reduced graph, and the expanded versions of the super-vertices. At any level of the recursion, our tighter conditions are once again used to decide whether the corresponding sub-floorplan to be generated is slicible. In this paper, the method proposed for floorplan optimization has two major advantages: (i) it is simpler, as it uses a reduced graph for topology generation thereby inducing a much smaller search domain, (ii) it is likely to generate slicible floorplans without any pseudo-vertices for a larger set of input graphs than previous algorithms.

3. PRELIMINARIES

A rectangular floorplan (RFP) is essentially a rectangular dissection of a given rectangular section by isothetic line segments called cuts. The indivisible non-overlapping rectangles correspond to the functional modules. A floorplan is said to be slicible if it is obtained recursively by using through-cuts or slices only, otherwise it is nonslicible. A slicible RFP can be represented by a tree. Conventionally the circuit modules are assumed to be rectangular in shape and the junctions among such rectangles are assumed to be T-junctions only. Two floorplans having same rectangular graph are said to be equivalent.

A given a plane triangulated graph (PTG) G has a corresponding RFP F only under certain necessary and sufficient conditions [1, 4]; such an adjacency graph is called a rectangularly dualizable graph, or in short, a rectangular graph. These graphs have unique plane embeddings.

To determine a floorplan F for a rectangular graph G, the unique embedding of G is first extended by adding four external vertices r, b, l and u on four sides of G corresponding to the right, bottom, left, and top boundaries respectively of a floorplan of G. The exterior vertices of G are connected appropriately to the external vertices and the edges (u, r), (r, b), (b, l), (l, u) are added in order to form an extended rectangular graph E(G) (Fig. 2), which is also planar. A vertex in G adjacent to more than one vertex of r(G), b(G), l(G), u(G) is called a corner vertex. At most four vertices on the outermost cycle of G are chosen as corner vertices [4]. A corner vertex in G corresponds to a corner module of G. The four corner vertices in G need not always be distinct.

Next, G_d the geometric dual of E(G) (without considering the exterior face of E(G)) is determined and embedded rectilinearly to obtain a floorplan F. Since the outermost cycle of G_d is embedded as the bounding rectangle of the floorplan for

G, the four sides of this rectangle, denoted by West, South, East and North consist of the four sets of exterior vertices of G_d .

A path in G_d is a sequence of vertices such that the consecutive vertices in it are adjacent. A cut in the floorplan is a path in G_d between two exterior vertices on two opposite sides; the corresponding cut-set of edges in E(G) decomposes it into exactly two non-empty subgraphs G_l and G_r . The two sequences of vertices on the two sides of these cut-edges of G, called the boundary paths P_l and P_r of the cut, are essentially the new boundaries of the sub-floorplans on the two sides of the cut, for the subgraphs G_l and G_r , respectively.

A chord free path (CFP) [9] in G is a path $P = \langle v_1, v_2, \ldots, v_n \rangle$ where for all $i \neq j$: a) $v_i \neq v_j$ and, b) if $(v_i, v_j) \in G$, then |i-j|=1. If P is not CFP, then it has two vertices v_i and v_j such that |i-j|>1 and the edge (v_i, v_j) in G is called a chord of P. A chord (v_i, v_j) , i < j is called a maximal chord of P, if there is no other chord (v_k, v_l) where $k \leq i < j \leq l$.

A cut is chord free if both of its boundary paths are chord free. A proper slice in a floorplan is a cut which is chord free (therefore embedded as a straight line) and both G_l and G_r are rectangular. A cut is vertical (horizontal) if it is between North and South (East and West) sides. The cut-set in G corresponding to a slice in a floorplan is often referred to as a slice in G. Hence, a floorplan of a given G can be obtained in a top-down fashion by recursively finding slices among several possible cuts in the floorplan. For nonslicible floorplans, slices may not exist at some levels of recursion.

In a plane graph, a complex cycle of length n (or a complex n-cycle), denoted by C_n , is a cycle of n edges such that there exists at least one vertex in the finite region bounded by the cycle. A necessary condition for rectangular dualizability is that G must not contain any complex triangle. One of the earlier sufficiency conditions for existence of slicible floorplans, is that G has no complex 4-cycles. An example of a rectangular graph with complex 4-cycles, and its floorplan is illustrated in Fig. 1. A maximal C_4 (MC_4) is defined to be a C_4 which is not contained in any other C_4 of the rectangular graph, (eg. cycle 1,2,3,4 in Fig. 1). By definition, a MC_4 of a rectangular graph cannot contain another MC_4 . A C_4 can be either center-sliced or corner-sliced [9]. Due to rotation symmetry, there are four different corner-slicings of an MC_4 .

4. NEW STRONGER SLICIBILITY CRITERIA

Some of the known properties of slicible floorplans and the corresponding rectangular graphs, which are relevant to our new criteria for slicibility, are recapitulated below.

- (a)[4] Let G be a planar triangulated graph with corner vertices fixed. G admits a RFP if and only if E(G) contains no complex triangle.
- (b)[9] Let G be a planar triangulated graph which admits a rectangular floorplan. Let E_s be a vertical slice on G and G_l and G_r be two sub-graphs decomposed by E_s . If both boundary paths $P_l(E_s)$, $P_r(E_s)$ are chord free, then both G_l and G_r admit rectangular floorplans.
- (c)[9] Let F(G) be a slicible rectangular floorplan. Let $S = (e_1, \ldots, e_n)$ be a slice of F(G). The corresponding set of dual edges $E_{\bullet} = (e'_1, \ldots, e'_n)$ in G is a proper slice.
- (d)[9] The intersection of a proper slice E, and any C₄ is either empty or contains exactly two edges.

Our new result on slicibility is now presented in the theorem below.

Theorem 1 A rectangular graph G with n vertices, n >4, is slicible if it satisfies either of the following two con-

- its outermost cycle is a complex 4-cycle (C₄) and not all the four exterior vertices of it are required to be corners;
- its outermost cycle is not a C₄ and all the complex 4-cycles of G are maximal.

Proof: Consider an arbitrary rectangular graph G =(V, E). E(G) contains no complex triangle (C_3) . It is to be shown that if either of the above conditions is true, then there always exists a proper slice E_{\bullet} through G.

For a given E(G), the corner vertices are fixed. If G contains a cut-vertex v_c , E_o can be the set of edges incident to the left (or right) of v_c . If there is a vertex $v \in G$ which occupies two corners (non-distinct), simply let E_s be the set of edges incident to v. This covers the first sufficiency condition of the theorem. Since the outermost cycle is a complex 4-cycle and not all four exterior vertices are not required to be corners, one of them is assigned two corners.

Thus the remaining graphs are those with distinct corners in E(G) and G contains no cut vertex. For this purpose, the vertices of E(G) are labeled using a procedure similar to that used in [9]:

- Delete the vertices u(G), l(G), and b(G) and their incident edges.
- Starting from r(G) as the root vertex, traverse the remaining graph in a breadth-first (BFS) manner. Label a vertex v at level i in the BFS tree as v^i .

The graph is now redrawn so that vertices on the same BFS level are vertically aligned (Fig. 2). It was shown in [9] that if the graph does not contain any C_4 , then it admits a slicible floorplan. Considering the above BFS ordering, now the second condition of our theorem is proved by showing that it is possible to construct a proper slice even in the case when complex 4-cycles exist, provided all of them are maximal. In this construction procedure, for each proper vertical slice we consider only the maximal chords. Moreover, a sequence of slices from right to left s constructed, so that the right boundary path of any slice is always chord free. From planarity of the rectangular graph, since chords are pairwise non-crossing, local modifications around a maximal chord (details given later on) are used for such construction. For the purpose of establishing our stronger condition, w.l.o.g. it suffices to consider only complex 4-cycles with a single vertex within it. Any subgraph within a complex 4-cycle can always be replaced with a super-vertex and our results apply equally to those cases too.

Let E(i, j) denote the set of edges between levels i and jand let the vertices at level i be labeled $v_1^i, \ldots, v_{n_i}^i$. Then, a vertical slice through E(G) is simply given by

 $S_0 = E(i, j) - \{(u(G), x) \mid x \in V\} - \{(b(G), y) \mid y \in V\}.$ Its boundary paths are given by $P_r(S_0) = (v_0^i = u(G), v_1^i, \dots, v_{n_i}^i, v_{n_i+1}^i = b(G)); \quad P_l(S_0) = (v_0^j = u(G), v_1^j, \dots, v_{n_j}^j, v_{n_j+1}^j = b(G)).$

In the proof below, consider j = i+1. A number of possible cases may arise when all complex 4-cycles of G are maximal. Case 1. Isolated set of maximal C_4 s in G.

Case 1.1. All the C_4 s interior to G.

Consider the BFS representations for a C_4 interior to G(Fig. 3) and the slice S_0 . Then, the corresponding segments of P_r and P_l are given by $P_r(S_0) = (v_k^i, v_{k+1}^i, \ldots, v_l^i); \quad P_l(S_0) = (v_p^{i+1}, v_{p+1}^{i+1}, \ldots, v_q^{i+1}).$

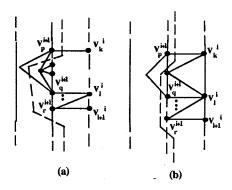


Fig. 3: Proper slice in a graph with isolated C_4

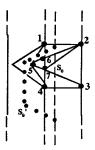


Fig. 4: An example of chord detour

A. As illustrated in Fig. 3a, the cut S_0 has a C_4 on its left. Let v_r^{i+1} be the topmost vertex in the BFS ordering mentioned above, which is adjacent to v_{l+1}^i . In order to construct a proper slice, consider a detouring operation w.r.t. the maximal chord (v_p^{i+1}, v_q^{i+1}) on left of S_0 . The modified slice S_0' excludes those edges of S_0 which have left end-points in the range $\langle v_{p+1}^{i+1}, \dots v_{p+1}^{i+1} \rangle$, and includes the maximal chord itself, the edge $(v_p^{i+1}, v_{p+1}^{i+1})$, the edges between levels i+1 and i+2 with right endpoints in the range $\langle v_q^{i+1}, \dots v_r^{i+1} \rangle$, and the edge $(v_r^{i+1}, v_{r+1}^{i+1})$, thereby ensuring a CFP on the left of the S'_0 . For example, in Fig. 4, the edges (1,2), (2,6), (2,7), (3,7), and (3,4) in S_0 are replaced by the edges (1,2), (1,6) and (1,4) to obtain S_0 . It is claimed that such local modifications do not result in the creation of any new chord on the right of S_0' .

For the sake of contradiction, let $P_r(S_0)$ have a chord (α, β) . Now the following cases may arise:

- A.i) Both α and β are at level $i:(\alpha,\beta)$ is an edge of $P_r(S_0)$, which became a chord when the maximal chord was detoured. This implies that there is a chord (v_k^i, v_{l+1}^i) , but since a sequence of vertical slices from right to left is being obtained, this would have been a chord in the previous iteration between levels i-1 and i. If i=1, then the presence of this chord implies the existence of a C_3 in E(G).
- A.ii) Both α and β are at level i+1: By construction of S_0 , both of these vertices must be included in $P_r(S_0)$ due to the local modification. This implies the existence of a C_3 in G.
- A.iii) α is at level i and β is at level i+1: The only possibility is that $\alpha=v_k^i$ and $\beta=v_q^{i+1}$, but this implies the existence of a $C_3 = (v_k^i, v_p^{i+1}, v_q^{i+1})$ in G.

B. Now, consider the alternative BFS representation (Fig. 3b). The cut S_0 intersects the C_4 and has a maximal chord on its left. To construct a proper slice S_0 , a similar detour operation w.r.t. the maximal chord on left of S_0 is performed. Once again, if S_0 happens to have a chord (α, β) , the following possibilities may occur.

- B.i) Both α and β are at level $i:(\alpha,\beta)$ became a chord of $P_r(S_0')$ when the maximal chord was detoured. This is similar to Case A.i above and is handled in the same manner.
- B.ii) Both α and β are at level i+1: By construction of S'_0 , and from planarity of the graph, such a chord cannot exist
- B.iii) α is at level i and β is at level i+1: By construction of S'_0 , and from planarity of the graph, such a chord cannot exist in this case also.

Case 1.2. Some C_4 s along the outermost cycle of G. In this case, w.l.o.g. assume that the vertices v_k^i , v_p^2 and v_q^2 are at the three corners of G. It is clear to see that the detour operations of Case 1.1 are identically applicable in this case, and hence a proper slice can be constructed through the C_4 . Extending our reasoning to the general case, it can be inferred that if G contains an isolated C_4 having at most three exterior vertices of the latter along its outermost cycle, then a proper slice can be constructed through the C_4 .

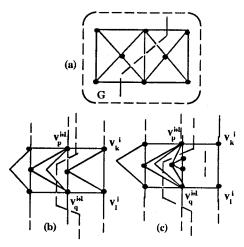


Fig. 5: Proper slices in a graph with two C₄s sharing an edge

Case 2.1. Two C_4 s sharing an edge. Case 2.1.1. Both C_4 s interior to G.

Two BFS representations exist for this case, as shown in Fig. 5. Consider Fig. 5b. Slice S_0 is intersecting the C_4 on the right and has a chord on left of it. Application of the slice detour operation results in S_0 . By same reasoning as in Case B of 1.1 above, it can be shown that no chord exists on either side of S_0 . However, the proper slice S_0 is special, as it corner slices both the C_4 s simultaneously.

For the alternate BFS representation of Fig. 5c, following the reasoning of Case A of 1.1 above, a proper slice can be obtained which essentially corner-slices both the C_4 s simultaneously.

Case 2.1.2. One or both C_4 s sharing some boundary vertices and / or edges of G.

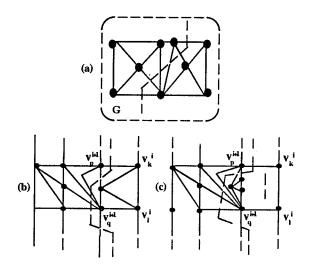


Fig. 6: Proper slice in a graph with two C₄s sharing a vertex

Let us assume w.l.o.g. that three exterior vertices of one of the C_4 s are at the corners of G. Then, by reasoning identical to those of Case 1.2, it is clear to see that a proper slice can be obtained which corner-slices both the C_4 s simultaneously.

If G contains only the two C_4 s sharing an edge (Fig. 5) then also a proper slice can be constructed through G.

Case 2.2. C_4 s sharing a vertex.

Case 2.2.1. Both C_4 s interior to G.

Consider the BFS representation in Fig. 6. The cut S_0 which detours a chord is a proper slice by similar reasoning as above. This essentially corner slices both the C_4 s.

Case 2.2.2. One or both the C_4 s have some vertices and/or edges on the outermost cycle of G.

As shown in Fig. 6, a proper slice can be obtained through both the C_4 s. If the boundary vertices of the C_4 s are such that the vertices v_1^{i+1} and v_1^{i+2} are adjacent to t(G) in E(G), then bipartitioning the graph using S_0' yields an $E(G_l)$ with a C_3 . Hence, in this case, slicibility of G cannot be guaranteed.

Finally, in our above analysis, since the modified slice includes the maximal chord that is detoured, there is a possibility of introducing a chord to the left of the modified slice. If there is a chord between any two vertices in level i+2 which are connected to v_q^{i+1} , it implies the presence of a C_3 in G. Alternatively, a chord may exist to the left of S_0^i between two vertices in level i+2 either of which is also connected to the vertices v_{q+1}^{i+1} , v_{q+2}^{i+1} , ..., v_r^{i+1} . In such a case, an alternative proper slice through G can be constructed by starting the BFS traversal of E(G) from l(G) (Fig. 7). If for a particular assignment of corners, it is not possible to construct a vertical slice through G at some stage, a horizontal slice can always be constructed through it. Blocking of both horizontal and vertical slices implies the presence of a nested C_4 , which contradicts the second condition of Theorem 1 [11].

For a small set of E(G)s, however, construction of a proper slice through it may not be possible; such examples are shown in Fig. 7. It is easy to show that for such E(G)s, slight alteration of the corners of the E(G) will always make G slightle

In general, however, G may contain a combination of all the above cases. In all the instances, extending the above

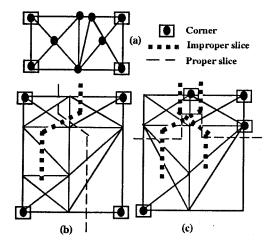


Fig. 7: Some interesting cases

discussions, it is easy to show that a proper slice can always be constructed.

Observation 1 For a rectangular graph G containing nested C4s, slicibility cannot be guaranteed by the above criteria.

5. UNIFIED TOPOLOGY GENERATION AND **OPTIMAL SIZING**

The new result on slicibility is utilized to obtain a unified method for topology generation and optimal sizing. The method starts with an input rectangular graph G and checks whether it satisfies the first condition of Theorem 1. Then it finds all the C_4 s in it, and selects the MC_4 s in them. The subgraph within each of them is then replaced with a supervertex to obtain a reduced graph \tilde{G} . The information stored for a super-vertex are its subgraph and the nesting of C_4 s in it. The unified floorplan optimization method AO_FP^* of [3] is then applied to \tilde{G} with the addition of recursive checking of condition 1 in Theorem 1 for the subgraphs G_l and G_r .

For topology generation, an AND-OR graph search is applied as in [3]. Each OR node represents the several ways of splitting a rectangular graph (or its subgraph), and each AND node represents an actual split. For each leaf node, since the set of implementations are known, they are used to estimate the dimensions of any composite module (which is a part of the RFP) corresponding to a subgraph.

A leaf may be a simple vertex or a super-vertex. In case the leaf is a super-vertex, its corner vertices are first determined, and the unified method is recursively applied to the corresponding subgraph to determine the set of implementations for it. During recursive bipartitioning, a minor alteration is required in selecting one of the possible slices at an OR-node; the slice with the best score among those for which the two corresponding subgraphs satisfy Theorem 1, is chosen and then slices in the subgraphs are searched for. In the event of failure to find such a slice, the one with the best score is selected and both slices as well as Z-cuts [3] in the subgraphs are looked for.

At the end of the search procedure at the topmost level of recursion, as in [3], a marked tree is produced, each node of which represents either some cut or some basic rectangular block. This marked tree corresponds to the floorplan

tree T_F corresponding the obtained topology. A bottom-up processing is now performed using T_F to obtain an optimal implementation of the topology generated.

By applying our new results of Theorem 1 to topology generation and sizing of RFPs, a substantial reduction in the search space is attained. Moreover, since slices are used for a larger set of input rectangular graphs, the bottom-up sizing procedure is very simple.

Complexity: The time complexity for finding all C_4 s is $O(n \log n)$, n being the number of vertices in the rectangular graph, as shown in [9]. The complexity for the AND-OR search method is difficult to analyze but that of the bottomup sizing is polynomial in n in all slicing and most of the nonslicible cases.[3].

Currently implementation of this new algorithm is in progress and experimental results will be available shortly.

The Algorithm

Algorithm optplan

Input: A rectangular graph G;

Output: A floorplan topology for G and an irreducible set of implementations for it.

begin

find all C_4 s in G;

replace interior subgraph of each MC4 with a super-vertex to obtain the reduced graph \tilde{G} ;

for each super-vertex, preserve corresponding subgraph and the list of C_4 s and their nestings in it;

 $AO_FP(\tilde{G})$

(* finds optimal implementations for topology obtained *) find_size(\tilde{G});

 $\mathbf{end}.$

procedure $AO_FP(G')$

begin

if G' satisfies Theorem 1 then

 $AO_{FP_{general}^{**}}(G');$ (* only slices to be looked for in \tilde{G} *) else $AO_{FP_{general}^{**}}(G');$

(* both slices and Z-cuts to be looked for in \tilde{G} *)

The subroutines AO_FP** and AO_FP** are the same as the AO_FP* [3]; in the former, only slices are used, while in the latter, slices and/or Z-cuts are used. During the topology generation phase, when a leaf node corresponding to a super-vertex is encountered, a recursive call to AO_FP is initiated on the subgraph corresponding to the super-vertex. If this subgraph has complex C_4 s, then their interior portions are again reduced to super-vertices at that level of nested recursion.

5.2. Example

Fig. 8a shows a rectangular graph G having three C_4 s viz., (11,12,14,21), (16,17,18,23) and (25,26,27,28), of which the first two are MC_4 s. In order to apply our algorithm to this graph, first the nested C_4 (25,26,27,28) is replaced with a super-vertex 24 to have a reduced graph \hat{G} as shown in Fig. 8b. Fig. 8c shows a BFS representation of E(G) and a proper slice through it, corner slicing the C_4 (16,17,18,23). Corresponding P_l and P_r are observed to be chord free.

At the top level of recursion, using AO_FP**, let a leaf node n_s of the AND-OR graph correspond to a super-vertex, and hence a next level of recursion initiates at n_a . If the subgraph corresponding to n_s is a C_4 with all four exterior vertices as distinct corners, $AO_FP^*_{general}$ is applied to it followed by the bottom-up function find_size(). On completion of the execution of $find_size()$ at node n_s , control returns back to $AO_FP^{**}_{slim}$ for the \tilde{G} and continues in that manner.

6. CONCLUSION

Even though complete characterization of Inherently Nonslicible floorplans is still an open problem, our work in this paper is one step forward to revealing the mystery. If the input graph contains only maximal complex 4-cycles, our algorithm always generates a slicible floorplan. For other types of input graphs, however, our method may use Z-cuts to obtain a general floorplan. Optimal sizing has been incorporated in our method so as to generate area-optimal floorplans. The notion of super-vertices to reduce the input graph and the doubly recursive approach need to be studied further for improvement.

REFERENCES

- J. Bhasker and S. Sahni, "A Linear Algorithm to find a Rectangular Dual of a Planar Triangulated Graph", Proceedings 23rd ACM/IEEE Design Automation Conference (DAC), pp. 108-114, June 1986.
- [2] P.S. Dasgupta, S. Sur-Kolay and B.B. Bhattacharya, "VLSI Floorplan Generation and Area Optimization using AND-OR Graph Search", Proceedings 8th International Conference on VLSI Design, pp. 370-375, Jan 1995
- [3] P.S. Dasgupta, S. Sur-Kolay and B.B. Bhattacharya, "A Unified Approach to Topology Generation and Area Optimization of General Floorplans", Proceedings IEEE/ACM International Conference on Computer Aided Design (ICCAD), pp. 712-715, Nov 1995, San Jose, CA.
- [4] K. Kozminski and E. Kinnen, "Rectangular Dual of Planar Graphs", Networks, 15, No. 2, pp. 145-157, 1985.
- [5] R. Otten, "Efficient Floorplan Optimization", Proceedings IEEE International Conf. on Computer Design (ICCD), pp. 499-502, 1983.
- [6] S. Sur-Kolay and B.B. Bhattacharya, "Inherent Nonslicibility of Rectangular Duals in VLSI Floorplanning", Lecture Notes in Computer Science, No.338, Springer-Verlag (Berlin), pp. 88-107, 1988.
- [7] S. Sur-Kolay and B.B. Bhattacharya, "On the family of Inherently Nonslicible Floorplans in VLSI Layout Design", Proc. IEEE International Symp. on Circuits and Systems (ISCAS), Singapore, pp. 2850-2853, Jun 1991.
- [8] L. Stockmeyer, "Optimal Orientation of Cells in Slicing Floorplan Designs", Information and Control, 57, pp. 91-101, 1983.
- [9] K.H. Yeap and M. Sarrafzadeh, "Sliceable Floorplanning by Graph Dualization", SIAM Journal on Discrete Mathematics, May 1995.
- [10] K.H. Yeap and M. Sarrafzadeh, "A Unified Approach to Floorplan Sizing and Enumeration", *IEEE Trans. on CAD*, Vol. 12, No. 12, pp. 1858-67, 1993.
- [11] P.S. Dasgupta and S. Sur-Kolay, "A Stronger Condition for Slicibility of Rectangular Graphs", manuscript, November 1996.

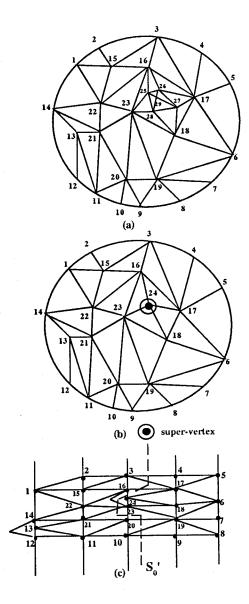


Fig. 8: (a) A graph, (b) its reduced form,(c) BFS ordering of the reduced graph