Low Power Signal Processing Architectures for Network Microsensors

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Abstract - Low power signal processing systems are required for distributed network microsensor technology. Network microsensors now provide a new monitoring and control capability for civil and military applications in transportation, manufacturing, biomedical technology, environmental management, and safety and security systems. Signal processing methods for event detection have been developed with low power, parallel architectures that optimize performance for unique sensor system requirements. Implementation of parallel datapaths with shared arithmetic elements enables high throughput at low clock rate. This method has been used to implement a microsensor spectrum analyzer for a 200 sample/s measurement system. This 0.8µm CMOS device operates with a 1µA drain current at a 3V supply bias.

I. Introduction

New monitoring and control information services are being developed with distributed, low power, wireless microsensors. A wireless microsensor network may be deployed rapidly and without modification to large structures and systems. Also, wireless sensors may be applied in areas where volume and mass constraints limit the application of conventional wireline interface sensors. This new wireless network architecture has applications in a broad spectrum of commercial and military applications ranging from clinical medicine, precision manufacturing, and transportation to battlefield perimeter security and shoreline reconnaissance.

Low Power Wireless Integrated Microsensor (LWIM) technology provides a distributed information system based on microelectromechanical systems (MEMS). The LWIM microsensor network transfers data from distributed sensing nodes to a base station through micropower, short range RF wireless links. Primary LWIM applications require sensor nodes powered by compact battery cells. Total average system supply currents must be less than 30µA to provide long operating life from typical compact Li coin cells. Low power, reliable, and efficient network operation is obtained with intelligent sensor nodes that include sensor signal processing, control, and a wireless network interface[1]. The signal processor described here can supply a hierarchy of information to the user ranging from a single-bit event detection, to power spectral density (PSD) values, to buffered, real time data. This programmable system matches its response to the power and information requirements. Distributed network sensor devices must continuously monitor multiple sensor systems, process sensor signals, and adapt to changing environments and user requirements, while completing decisions on measured signals. Clearly, for low power operation, network protocols must minimize the operation duty cycle of the high power RF communication system.

Low power sensor signal processing must be provided for continuous monitoring operation of remote, autonomous sensors. For this autonomous operation, an event driven network protocol has been developed. The associated event detection method relies on a single chip low power sensor spectrum analyzer. This DSP datapath system has been optimized for low power at both the system architecture level and the design implementation level. The spectrum analyzer system (with architecture shown in Figure 1) is implemented in 0.8µm HPCMOS with 45,000 transistors. Signal processing rate is set by the bandwidth of typical

![Figure 1. Low power sensor signal processing system. This architecture provides a continuous, adaptive spectrum analyzer function for monitoring of wide dynamic range, wide bandwidth microaccelerometer signals. The power-efficient spectrum analyzer operates continuously, allowing high power control and wireless network interface systems to rest in a sleep state.](image)
sensor systems. For typical seismic vibration sensing, this bandwidth is less than 100Hz. This device operates with a 1μA drain current at a 3V supply bias.

II. Low Power Network Sensor Signal Processing

Optimal, low power system operation can be obtained by operating only the essential sensor and signal processor systems while maintaining the microcontroller and all other components in a sleep state. Spectral analysis for LWIM nodes employs parallel, low clock rate, low bias voltage, dedicated datapath signal processors. This method accommodates the limited power available to a remote, wireless node.

The signal processor datapath elements compute power spectral density (PSD) values for selected bands identified adaptively by the user. PSD outputs are compared with spectral weights also provided by the user. A decision is made, therefore, on the average of many data records and on the spectral character of this record. Parallel operation provides high throughput, while low clock rate minimizes power. It is important to note that this system permits the node to incorporate a high performance, high peak power dissipation microcontroller that operates at a low duty cycle. Most importantly, the data path and threshold comparator operate continuously at low power, waking the processor from a sleep state only when a suspected threshold excursion is observed.

A custom DSP system with programmable filter coefficients is required for complex LWIM applications. The typical low frequency (1 - 50Hz) and relatively long duration events (1 - 100 seconds) that LWIM nodes must detect determine a set of unique characteristics. The DSP must exploit these characteristics to permit continuous low power operation. First, the low sampling rate (resulting from band-limited sensor response) allows the DSP unit to operate at low clock frequency (less than 100 kHz). Second, by taking advantage of slowly changing sensor PSD spectra, the DSP may reconfigure itself and reprocess the sensor signals in the event of overflow. This relaxes requirements on word length at the expense of complexity. However, VHDL-based design methods along with standard cell physical layout generation time have allowed short development cycles for this complex system.

III. System Architecture

The sensor spectrum analyzer is supplied with an 8-bit word from the sensor interface Σ-Δ ADC converter. This word is supplied to 8 parallel channels of a band-pass filter bank for spectrum analysis (see Figure 2). The output of each channel is squared and accumulated using a sum-of-squares (SSQ) circuit. After sufficient accumulation (averaging), the sum-of-squares values are then compared with a set of eight programmable threshold values to identify an excursion of measured PSD above stored thresholds in any of the 8 filter bands. Thus, sensor spectra are continuously monitored in each band. Threshold excursions are a sensitive and robust event detection method and may be used to trigger operation of high peak power node subsystems (that are maintained in a low power sleep state until needed). Also, upon request from a user, the LWIM node may supply a hierarchy of information, the 8 threshold binary values, the sum-of-squares values of each channel, or buffered, real time data. Thus, this sensor signal processing method provides a level of information that is scaled properly to the user requirements and to power level.

IV. Low Power Sensor Filter Architecture

The low power sensor application presents a unique design problem with respect to the choice of filter type (FIR or IIR) and the word length. For typical microsensor (accelerometer) PSD analysis, over 100 taps may be required for FIR filters. In contrast, IIR filter systems offer the advantage of reduced complexity. A typical 6th order IIR filter, in this system, requires 6 registers to store state variables and another 6 registers to store coefficients. In contrast, the FIR filter will require large register banks for programmable operation. The static power dissipation is also reduced in our IIR filters since the total number of transistors is less than that of equivalent performance FIR filters. Further, dynamic power dissipation is reduced primarily due to the reduction in the number of required multiplications. The design challenge for IIR filters is their performance sensitivity to finite word length. The complexity associated with implementation of feedback within the IIR filter systems have been addressed by our design approach.

The fixed point LWIM signal processor suffers from finite word length limitations that introduce quantization error
for sensor signal and filter coefficients, and truncation error when feedback is used in filter architecture. While the quantization error remains, the effect of truncation error can be reduced by cascading several stages of IIR filters.

Overflow due to finite word length constraints is addressed by re-scaling of filter input. First, for events of interest having a long duration (10^3 - 10^7 samples), overflow indication may be used to scale the filter input and output, while still capturing an event. For abrupt events, data buffering must be included (see Figure 1). Here, when overflow occurs, the buffered data will be scaled and processed.

Although the use of buffers improves the reliability of the entire DSP system, reprocessing of data reduces power efficiency in terms of power consumption per valid DSP output byte. Thus, minimizing the overflow probability is desirable. Increasing internal word length of the datapath and proper scaling of the filter coefficients are two possible options that can be taken to reduce the chance of getting overflow. Since typical events are short, the size of the buffer can be small as well, and the DSP unit can quickly return to process new data.

It is obvious that the buffers should hold as many bytes of data as is needed to generate one sum-of-squares output. If the buffer length is excessive, (or the sum-of-squares output is the result of a long averaging period) then a short duration event yields a small contribution to an average signal and may be “averaged out” and may not be detected. However, if the DSP output is based on a short sampling interval, then signal-to-noise is degraded. The optimal length of input depends on the duration of the events that are being detected. Thus it is application specific. With the design described here, the DSP unit can be designed in such a way that it is programmable for different input intervals for one SSQ output.

V. Programmable Low Power Filter

For the LWIM specific DSP datapath, two general rules are established to guide the design. First, since power consumption is the primary concern, area is traded for low power, such as reducing switching activity[2]. Second, because of the low data rate of sensor output, most of the arithmetic units and registers can be shared. As a result, silicon area cost can be minimized.

The front end of the DSP unit is essentially an updown counter. It is the last stage of an 8-bit sigma-delta A/D converter[3]. This stage consists of three major parts, a clock divider, a unidirectional counter, and the actual updown counter. The task of the clock divider is to divide the system clock to the desired sampling rate while the unidirectional counter determines the resolution of the A/D converter. The updown counter then generates an 8-bit unsigned digital word which is further converted to 2’s complement representation with an offset of 128, for the purpose of having the filter output centered around zero.

The next stage is the 8-channel IIR filter bank. In order to reduce the effect of truncation error, a cascade structure of two 2^{nd} order IIR filters is used. Two configurations are being investigated with direct performance comparison. The first configuration is the conventional direct form II realization (Figure 3a). A simple method for management of the state variables in this form of IIR filter is to shift the first order delay states into the second order delay states and then shift the new states into the first order delay. However, parallel shifting creates high switching activity at transistor nodes and thus high dynamic power dissipation. In accordance with the first design rule discussed above, a finite state machine is used to lower the transistor switching activity. Additional silicon area is used to multiplex the state variables to the multiplier. The second configuration uses two 2^{nd} order FIR filters and a subtractor (Figure 3b). Filter coefficients are multiplied by the input data and the results are accumulated. The subtractor performs subtraction (for feedback) between the FIR filter outputs. The first FIR filter acquires input data while the second FIR acquires the subtraction result for feedback. The first method consumes less area while the second method offers reduced area and complexity.

![Figure 3. (a) IIR filter in Direct Form II. (b) IIR filter realized with two FIR filters and a subtraction unit.](image)

An important feature of the LWIM signal processor architecture is the sharing of arithmetic units (shown in Figure 4). One multiplier and two adders in the filter are shared by all 8 channels. One of the two inputs to the multiplier is fed by the output of a coefficient memory block, the other is connected to the state variable or sensor data registers through a multiplexer. A triggering signal is used to place coefficient and data pairs at the multiplier input. Also, filter bank activity is set to be idle until the conversion done signal from the A/D converter starts a new process. By sharing these arithmetic units, the silicon area can be dramatically reduced in comparison to conventional multiplier chains.
Programmability of the LWIM filter bank is accomplished by providing a coefficient register stack. However, this programmability can introduce both area and power cost. In order to take the advantage of rapid standard cell design, the coefficient storage block is based on D type flip flop register cells (see Figure 5). This choice of structure for this block is motivated by the first design rule—optimizing power at the expense of area. Also, the design exploits the system operating characteristic that coefficient update will occur infrequently and may be implemented with a serial-in shift register. However, power must be minimized by parallel access of coefficients. For coefficient output, each coefficient is connected to an output bus by a tri-state buffer. The buffer is controlled by a one bit wide and 96 bit long shift register whose length is equal to the total number of coefficients[4]. Thus, there will only be one bit high in the one bit shift register and therefore only one coefficient can pass to the output bus through its tri-state buffer. For a filter bank of eight 4th order IIR filters, a total of 96 coefficients is needed. The dynamic power of this structure is less than 1% of that for a simple parallel shift register of coefficients. The cost of this power reduction is, of course, the area for the tri-state buffers and the one bit shift register. The programmability of the filter bank is realized through downloading of coefficients from the user.

The sum-of-squares (SSQ) unit design also is based on arithmetic unit sharing. Rather than in parallel, the SSQ of the eight channels are calculated in series to permit sharing of the multiplier and accumulator. Eight separate register words hold the intermediate and the final SSQ values of the eight channels respectively. At the end, the final SSQ values are placed consecutively on the output port to the comparison unit at 10kHz.

The last stage of the signal processing system is a comparison block. The threshold values are shifted along with the filter coefficients into the same storage block. An 8-bit length shift register controls the tri-state buffers that connect the threshold registers to an output port of the comparison block. If any SSQ value is greater or equal to its corresponding threshold value, an interrupt bit is set to request attention from the controller for this event.

The filter structure described above and the carefully prepared coefficients form a complete digital filter. Three 10 Hz wide bandpass filters with passband center frequency located at 5 Hz, 25 Hz, and 45 Hz are elected as test cases with an input word rate of 100Hz. Sinusoidal inputs over a range of frequencies are used to characterize the filters. The frequency responses of all three channels are shown in Figure 6.
VI. System Implementation

LWIM signal processing system design has leveraged CAD tools extensively to assist the design process and speed up the route to silicon. This enables focus on algorithm and system level design with rapid verification of low power design concepts. VHDL behavior codes describe system architecture and functionality and operation of each individual module in the datapath. RTL and gate level syntheses are completed with Synopsys tools. The design is implemented using the Synopsys 0.8 mm CMOS (HP26G) standard cell library. Finally, physical layout generation is assisted by Cascade Design Automation tools. Operation of the first LWIM spectrum analyzer system (see Figure 7) verifies low power operation. At a sample rate of 200 samples/sec, a Σ-Δ clock rate of 100kHz, the supply current drain was less than 1μA at a 3V supply bias.

Figure 7. The spectrum analyzer system is implemented in 0.8μ HPCMOS with 45,000 transistors. This system operates with a 1μA drain current at a 3V supply bias at 200 sample/sec processing rate.

VII. Conclusion

In summary, a low power spectrum analyzer for sensor measurement has been developed. The system architecture exploits the unique characteristics of distributed sensor systems to provide low power operation. Design of this programmable DSP system employs sharing of arithmetic units to minimize chip area. Finally, operation of a complete chip demonstrates feasibility of this architecture for operation below 3 μW for compact, distributed sensors.

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References


