Evening Panel: Low Power Design without Compromise

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Panelists:

Pari Assaderaghi     IBM, Yorktown Heights, NY
Francky Catthoor     IMEC, Belgium
Frank Fox            DEC, Hudson, MA
Dave Greenhill       Sun Microsystems, Mountain View, CA
Deo Singh            Intel, Santa Clara, CA
Jim Sproch           Synopsys, Mountain View, CA

It is mid 1998. The Speedy Microsystems design team is discussing a memo they have just received from Marketing about their next generation machine due to tape out in 2000, a 1.5V, 1GHz, 100 watt, 40 million transistor superscalar microprocessor with multimedia extensions to be fabricated in 0.18um CMOS. Only one problem. Marketing has just announced a major push into Network Computers, and all of a sudden the power budget has dropped to 4 watts. Including the multimedia extensions and an on-chip radio. Worse yet, a major customer has just invented a 50mW color display and is threatening to cancel its $1 billion order unless Speedy can deliver a 100mW processor in 18 months. Not only that, Marketing wants to continue pushing forward at the high end because there has been explosive growth in the server market.

Frustrated with their own ability to meet these requirements, Speedy has hired a team of experts to figure out how to meet these power budgets while giving up the least performance. The team has had a brief organizational meeting at which they have decided to break the problem into two parts. First, each expert will give his view on how best to solve Speedy’s problems assuming all the technology that has been reported is readily available and carries no risk. Second, the group is going to collectively decide, with the help of the audience, what constitutes an acceptable level of risk for Speedy and what can realistically be accomplished in the next 18 months. Come listen in on the first technical meeting of this team and help them try to meet Speedy’s goals.

Fari Assaderaghi (IBM)

Technology provides a great leverage in the power/performance equation. The targeted power and performances impact the design choices all the way down to the transistor level. Even though conventional bulk technology offers solutions such as multiple threshold voltages, and active substrate biasing, the best technology approach is utilization of SOI. Here, a 3X reduction in power can be made without a sacrifice in speed by just remapping the design from bulk to SOI. An even greater advantage can be realized by specific circuit design for SOI. To drastically reduce the power, Dynamic Threshold MOSFET (DTMOS) is the ultimate technology vehicle, not surprisingly best suited for SOI!
Francky Catthoor (IMEC)

Much of the power to be gained still in the future will not be technology/circuit based but related to the system and compilation stages. Data transfer and storage in processors become integrated on-chip (also the L2 cache) so the power associated with these components is becoming even more dominant. The circuit techniques used in memories and buses are reaching the limit in CMOS (with limited internal voltage swings). Especially in multi-media applications, much power improvement can still come from how to compile the given application on the available memory and bus hierarchy.

Frank Fox (DEC)

There is no magic -- it all comes down to $CV^2 f$. Capacitance can be reduced by a factor of four by using SOI, low k dielectrics, dense custom layout, and power-conserving floorplanning. Halving Vdd reduces power by another factor of four. Halving clock frequency and aggressive use of clock gating will reduce power by yet another factor of four. So power consumption can be reduced from 100W to under 2W for a 50% reduction in performance. After that, the going gets tough. The performance will drop by a further factor of seven to get to 100 mW.

Dave Greenhill (Sun Microsystems)

High performance machines and low power machines are completely different animals. Don’t even try to make them the same. Speedy needs to form a new design methodology to tackle low power, making compromises at all levels to meet the power budgets. High performance machines inherently waste power. They have deep pipelines and aggressive circuits. They often use techniques such as prefetching, prediction and speculative execution that improve performance at a significant power cost from wasted effort and logical support for these functions. Process technology is chosen for performance not for power efficiency. Speedy needs a new architecture, new logic design, new circuit design and new process technology.

Deo Singh (Intel)

Seriously consider dumping your Speedy stock options as quickly as possible! Recognize that marketing always exaggerates; what the customer can really live with is a 1 Watt processor. Speedy would like to exploit savings from SOI but rejects the idea because of low reliability in high volume manufacturing. Analysis of Speedy’s design techniques/methodology show that they consistently overdesign their processors and consistently waste power. Good microarchitecture/logic/ckt design techniques and CAD tools can reduce power by 10x without compromising performance, bringing the power down to 10 watts. Voltage scaling to 0.5 Volt will reduce power to 1 watt, but this requires new circuit techniques/families that are elegantly voltage scalable (minimal performance degradation).

Jim Sproch (Synopsys)

Low power CAD tools are here; they will help reduce power dissipation, but they are not a panacea. Power analysis tools can help guide the designers to better architectures and focus their efforts on parts of the circuit where the most opportunity for power reduction exists. Synthesis and physical design tools can all be power-savvy and thus help reduce circuit power dissipation. New clocking strategies, I/O signaling schemes, and power management techniques can further curtail power dissipation.