On the Power Dissipation in Dynamic Threshold Silicon-on-Insulator CMOS Inverter

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Abstract

The leakage current due to the parasitic PN junction diodes in SOI DTMOS (Dynamic Threshold Voltage MOSFET) inverter is reported. The additional power dissipation in DTMOS inverter due to the diodes is quantified through an analytical model and verified by MEDICI simulation. Power dissipation between conventional SOI CMOS and SOI DTMOS inverters is compared.

I. Introduction

Body-tied-to-gate DTMOS (Fig. 1) can be operated at low power supply while still maintaining a large drain current for high speed application, without introducing any extra amount of standby current, therefore it is suitable for low voltage VLSI applications.[1][2]. Performance of DTMOS ring oscillators based on both SOI and bulk wafers was reported. With 0.6V power supply voltage, propagation delays of 500psec in 101-stage oscillator using 0.33um SOI DTMOS[1] and 83.6psec in 61-stage oscillator using 0.22um N-channel and 0.26um P-channel bulk DTMOS[2] were achieved. Figure 2 shows the MEDICI[3] simulation results of $I_{ds}$ versus $V_{gs}$ characteristics of SOI DTMOS and conventional floating-body Non-Fully Depleted (NFD) SOI MOSFET. It shows that both a steeper subthreshold slope and larger current drivability are achieved in DTMOS for a given $V_{gs}$. Though advantages also exist in bulk DTMOS, SOI promises better performance. In SOI DTMOS, the junction capacitance is smaller than that of bulk device, and body current is restricted in lateral direction because of the buried oxide underneath the Si film. Thus, SOI DTMOS offers a smaller power-delay product than bulk DTMOS circuit using the same technology.

These advantages, however, do not come free. If DTMOS is connected in the pull-up/pull-down configuration such as in the inverter circuit, the power dissipation will increase. The static power dissipation increases due to the leakage of the forward biased body-source/drain PN junctions. The capacitance associated with the parasitic PN junction diodes also adds to the power dissipation during the switching. In this paper, we shall quantify the additional power dissipation in DTMOS gates due to the parasitic diodes, and compare the power dissipation of inverter circuit composed of different SOI devices.

II. Power Dissipation Model for DTMOS Inverter

a. Static Power Dissipation

Figure 3 shows the schematic of an inverter circuit consisting of P-channel and N-channel SOI DTMOS. The parasitic lateral bipolar inherent in the DTMOS will not turn on in the inverter circuit as it is not biased in the forward active mode, so in the following analysis only the two back-to-back parasitic diodes behavior of DTMOS is considered. When the input logic is low, both of the PMOS parasitic diodes $D_{p1}$ and $D_{p2}$ are forward biased by $V_{dd}$. As a result, there are two DC current paths as shown in Figure 3, one from $V_{dd}$ through $D_{p1}$ to $V_{in}$ (solid line), and the other from $V_{dd}$ through PMOS channel and $D_{p2}$ to $V_{in}$ (dotted line). Similarly, when the input is high, two current paths through NMOS parasitic diodes exist. Hence, the static power dissipation increases, compared with an inverter with conventional floating-body SOI CMOS, where the static power is mainly due to a small subthreshold leakage current of the device. The enhancement in the static power dissipation limits the range of the power supply of DTMOS circuit. Normally it should be kept below 0.7V to avoid large static body current.

The static power dissipation is the sum of the power due to subthreshold leakage and that due to the forward biased parasitic diodes. Since there are two conductive parasitic diodes during each half-cycle as mentioned above, the average power dissipation for each input cycle can be modeled as

$$P_{static} = V_{dd}I_{sub} + \left[ V_{dd}(I_{SN} + I_{SP})e^{V_{dd}/V_T} - 1 \right]$$

where $I_{SN}$ and $I_{SP}$ are the reverse saturation currents of the parasitic diodes associated with NMOS and PMOS respectively.

b. Power Dissipation During Switching

The power dissipation of DTMOS inverter circuit during switching consists of three components: charging and discharging power due to the load capacitance, short circuit power, and the parasitic diodes switching power.
The first component, \( C_d V^2 / T_e \), is identical for both conventional CMOS and DTMOS circuits. The short circuit power dissipation will not be discussed in this work as it is normally overwhelmed by the first component. The power due to parasitic diodes, however, is in addition to the total dynamic power dissipation in the conventional CMOS circuit. This extra amount, which is of interest to this paper, stems from the transient behavior of parasitic diodes in DTMOS.

Given a negative step input with fall time \( T_f \) (see Figure 3), the body potential follows the gate input so that diode \( D_{p1} \) and \( D_{p2} \) are gradually turned on while diode \( D_{n1} \) and \( D_{n2} \) are gradually turned off. Similar diodes turning on/off behavior takes place for a positive step input. All these behaviors during the switching lead to an additional power dissipation in DTMOS inverter. Figure 4 shows that the transient body current, which is essentially the sum of the back-to-back parasitic diodes current, is much larger than its steady-state value. The transient current through a diode can be modeled as

\[
I(t) = A \left( \frac{dQ_{dep}(t)}{dt} + \frac{dQ_{diff}(t)}{dt} + J_{qs}(t) \right) = A \left( C_j(t) \frac{dV_a(t)}{dt} + C_d(t) \frac{dV_a(t)}{dt} + J_{qs}(t) \right)
\]

where \( A \) is the junction area, \( dV / dt \) the input ramping rate, \( Q_{dep} \) the depletion charge and \( Q_{diff} \) the diffusion charge, \( C_j \) the depletion (junction) capacitance and \( C_d \) the diffusion capacitance, and \( J_{qs} \) the quasi-steady current density. The first two terms correspond to the charging current of the diode during the switching. In our case, \( Q_{diff} \) is small even if the parasitic diodes are forward biased, because the applied voltage \( V_a \) is low (not greater than 0.7V). \( J_{qs} \) is also negligible. Hence, the current through \( D_{p1} \), during the input rise/fall time can be simplified as

\[
I(t) = AC_j(t) \frac{dV_a(t)}{dt}
\]

where \( C_j(t) = \left[ qN_s \epsilon_e / 2 \left( V_a(t) - V_b(t) \right) \right]^{1/2} \), \( N_s \) being the doping concentration of the N-type body, \( V_b \) the PN junction build-in potential which is around 1V in this work. Assuming that the gate delay is zero and the output voltage changes rail-to-rail (from \( V_{dd} \) to 0 or from 0 to \( V_{dd} \)) linearly, then the current through \( D_{p2} \) during the input ramp time can be modeled as

\[
I'(t) = AC_j(t) \frac{2 x dV_a(t)}{dt} = 2AC_j(t) \frac{dV_a(t)}{dt} .
\]

Note that \( C_j(t) \) is not equal to \( C(t) \) as the voltages across \( D_{p1} \) and \( D_{p2} \) are different at the same time point. The total body current during the input rise/fall time is the sum of the two:

\[
I_{body}(t) = I(t) + I'(t).
\]

The NMOS body current has the same form as (3). The above model for body current during the input ramp time, though simple in form, offers a good estimation to the real situation as shown in Figure 4. Therefore, based on the same charge analysis approach, a power dissipation model for the parasitic diodes can be derived.

After the ramp time of the input, the transient current of the parasitic diode decays exponentially as shown in Fig. 4. For the modeling of parasitic diodes power dissipation, we may bypass the modeling of this part of the current, because it is taken care by the change in stored charges. Actually, it is more straightforward to model the power dissipation in terms of charge, as energy is simply the integral of charges over a certain range of voltage. Suppose a positive step with rise time \( t_r \) is applied to a diode, then the energy consumed during the switching is given by

\[
E = A \left( \int_{V_a}^{V_{dd}} Q_{dep} dV_a + \int_{V_a}^{V_{dd}} Q_{diff} dV_a + \int_{V_a}^{V_{dd}} J_{qs}(V) V_a(t) dt \right)
\]

As shown in Figure 3, when the input is ramping, the parasitic diodes \( D_{p1} \) and \( D_{p2} \) experience voltage change from \( 0 \) to \( V_{dd} \) and from \( V_{dd} \) to \( 0 \), respectively. Note that switchings from \( 0 \) to \( V_{dd} \) and from \( V_{dd} \) to \( 0 \) result in the same energy consumption. Thus, total energy consumed by the two parasitic diodes during the switching period of one cycle can be modeled as

\[
E_{diode} = 2 \left( A_p + A_n \right) \int_{V_a}^{V_{dd}} Q_{dep} dV_a = A_p + A_n \int_{V_a}^{V_{dd}} 2qN_s \epsilon_e \left( V_{bi} - V_a \right)^{1/2}
\]

where \( N_s \) is the doping concentration in the Si body and \( A_p \) and \( A_n \) are the junction areas of the parasitic diode associated with PMOS and NMOS, respectively. Consequently, the average power dissipation due to the parasitic diodes during switching is

\[
P_{diode} = E_{diode} / T_p
\]

where \( T_p \) is the cycle of the input signal.

Note that in modeling \( P_{diode} \) only \( D_{p1} \) and \( D_{p2} \) are considered. This is because the power dissipation due to \( D_{n2} \) and \( D_{p2} \) are similar in inverters composed of conventional NFD SOI CMOS and DTMOS. As it is hard to arrive at analytical expressions for the transient output voltage of the inverter circuit, in the following comparisons of power dissipation between the two types of inverter circuits, the power due to \( D_{n2} \) and \( D_{p2} \) will not be considered.

### III. Results and Discussions

A comparison of power dissipation models between DTMOS and the conventional CMOS inverter circuits is made in Table I with the differences highlighted. It is evident that the additional amount of power in DTMOS is dissipated on the parasitic diodes. In the following comparisons of circuit performance, the same device
technology is used. The parameters of SOI DTMOS and conventional SOI CMOS along with the circuit simulation parameters are listed in Table II. Figure 5 shows the different components of total power dissipation of the inverter circuit composed of those two types of devices. It demonstrates $P_{\text{diode}}$ in DTMOS is not negligible compared with that of the load capacitance ($P_{\text{dyn}}=C_L V_{dd}^2/T_p$). Moreover, due to the forward biased diodes associated with DTMOS, the static power dissipation increases exponentially with the power supply and outweighs $P_{\text{dyn}}$ when $V_{dd}$ approaches 0.7V. Thus, power supply beyond 0.7V is undesirable for DTMOS circuit.

Figures 6 and 7 show the MEDICI simulation results of the static currents through the power supply and ground in inverters composed of different types of SOI MOSFETs. In Figure 6, an obvious bending appears when the input voltage is low for the DTMOS inverter, demonstrating the additional amount of current through the PMOS parasitic diodes, compared with the case for conventional SOI CMOS inverter (dotted line). Similarly a DC current through the ground can be observed in Figure 7. The dashed line corresponds to the inverter with retrograde doped devices, which has a smaller static diode leakage than the inverter with uniformly doped devices. Retrograde doping, with peak situated at the interface of the Si body and the buried SiO₂, increases the doping concentration at the bottom of the body and consequently decreases the forward biased diode current. This scheme seems to be a benefit in addition to the punch-through prevention for short-channel devices. However, it is overshadowed by its side-effect which is the increase in the dynamic power dissipation of parasitic diodes. As shown in Figure 10, the parasitic diodes power dissipation during switching enhances with the increase in doping concentration at the bottom, because high doping in the Si film increases the body-source and body-drain junction capacitance, and consequently boosts up the diode transient current (Equation 1 and 2). To be power-conscious, doping profile engineering in the Si film is required in order to optimize the power dissipation and punch-through prevention.

Figure 9 shows the power-delay product of the inverter circuit composed of different SOI devices. The SOI DTMOS inverter with uniform doping devices displays the smallest product under low power supply. When the power supply approaches 0.7V, however, DTMOS inverter loses its advantage over conventional SOI CMOS due to the exponential increase in static power dissipation. Retrograde doping is necessary for punch-through prevention while unfavorable to power-delay product due to the large power dissipation of parasitic diodes during switching.

IV. Conclusions

The leakage current due to the parasitic diodes in SOI DTMOS inverter was reported. The additional power dissipation in DTMOS gates due to the diodes was quantified through an analytical and verified by MEDICI simulation. Power dissipation in the SOI inverter circuit based on conventional CMOS and DTMOS with different doping profiles in the silicon film was compared. The DTMOS inverter displays a smaller power-delay product than a conventional CMOS inverter when the power supply is below 0.7V. Doping profile engineering in DTMOS is required so as to minimize the power dissipation and prevent the punch-through problem as well.

References:

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<th>$P_{\text{static}}$</th>
<th>$V_{dd} \times I_{\text{sub}}$</th>
<th>$V_{dd} \times I_{\text{sub}}$ + $V_{dd} \times (I_{\text{SN}} + I_{\text{SP}}) \times \exp(V_{dd} / V_T)$</th>
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<td>$P_{\text{dyn}}$</td>
<td>$C_L \times V_{dd}^2 / T_p$</td>
<td>$C_L \times V_{dd}^2 / T_p$</td>
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<tr>
<td>$P_{\text{diode}}$</td>
<td>---</td>
<td>$E_{\text{diode}}/T_p$</td>
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Table I  Power dissipation models.

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<th>(W/L)₀ (µm)</th>
<th>(W/L)ₙ (µm)</th>
<th>Nₛ (N₀) (cm⁻²)</th>
<th>T₆0 (nm)</th>
<th>Tₚ (nm)</th>
<th>Cₛ (pF)</th>
<th>Input rise/fall time (ns)</th>
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<td>30/0.35</td>
<td>10/0.35</td>
<td>1.6x10¹⁷</td>
<td>7</td>
<td>150</td>
<td>0.1</td>
<td>0.5</td>
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Table II  Device and circuit parameters for MEDICI simulation.
Fig. 1 Cross-section of body-tied-to-gate SOI DTMOS.

Fig. 2 MEDICI simulation of $I_D$ versus $V_{GS}$ characteristics of N-channel SOI DTMOS and conventional SOI MOSFET.

Fig. 3 Schematic of SOI DTMOS inverter circuit.

Fig. 4 Model and MEDICI simulation results of transient current through the parasitic diodes of P-channel DTMOS in the inverter circuit.

Fig. 5 Different components of power dissipation in inverters with different SOI devices.

Fig. 6 MEDICI simulation of $I_{DS}$ in inverter with different types of devices.

Fig. 7 MEDICI simulation of $I_{GD}$ in inverter with different types of devices.

Fig. 8 Power dissipation of parasitic diodes in DTMOS inverter during switching.

Fig. 9 Power-delay product of inverter with different SOI devices.