The Impact of SOI MOSFETs on Low Power Digital Circuits

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Abstract Encouraged by the promising results of SOI device-based studies, CMOS on SOI has recently been suggested for the low power digital applications. In this paper, the crucial effects of SOI device characteristics on switching circuits is investigated, and the relative merits of SOI and bulk devices for circuit applications are compared. As a result, the impact of the floating body on SOI circuit performance and the related device solutions are discussed.

1. Introduction

Portable computers and wireless communication circuits are among the important applications that require low power electronics. Due to its superior subthreshold current characteristics and lower parasitic capacitances, SOI has shown great promise in these areas. However, the quantitative circuit advantages have not been carefully analyzed. In this paper, not only will the merit of SOI MOSFETs in digital circuits be addressed, but also the impact of parasitic effects will be examined in order to understand the underlying physical mechanisms involved. Finally, the choice of fully-depleted (FD), partially-depleted (PD) and body-tied (BT) SOI for digital circuits will be evaluated.

2. Floating body effect

The existence of a buried oxide results in the floating body and self-heating effects [1] in SOI. In floating body partially depleted (PD) SOI, the majority carriers generated by the impact ionization current accumulate in the neutral body and induce a threshold voltage reduction, resulting in the kink in the output characteristics [2]. In addition, the positive body voltage can turn on the source/body junction which induces a lateral bipolar action and an early breakdown, limiting the operating voltage. Two switching-related effects, the transient effect [3] and dynamic capacitive coupling, also influence digital circuits and their impact will be discussed in the next section.

3. Advantage of SOI on switching logic circuits

3.1 Speed: parasitic capacitances and \( V_{TH} \)

In switching logic, it is important that the \( V_{TH}/V_{DD} \) ratio be as small as possible to achieve good switching performance. For example, basic inverter analysis shows that the delay is given by [4]

\[
\tau_D = \frac{1}{2} \left( \frac{1-V_T}{2} \right) t_I + C_L \frac{V_{DD}}{2I_D},
\]

where \( V_T = V_{TH}/V_{DD}, \) \( C_L = (W_n+W_p)L/C_{ox} + \text{C}_{jn} + C_{jp}, \) and \( t_I \) is the input waveform transient. Two factors, \( V_{TH}/V_{DD} \) and junction capacitances, limit the speed. In order to evaluate the impact of the reduced junction capacitances in SOI, HSPICE SOI models, which lump the lateral BJT with MOS device by treating the substrate contact as the base of BJT, were used. Compared with bulk (same \( V_{TH} \) as SOI) inverter chains, SOI shows not only a speed improvement, especially for low power supply, but also lower power dissipation as shown in Fig. 1.

The other issue related to SOI based circuits is the design of \( V_{TH} \). As the power supply scales, \( V_{TH} \) has to scale to maintain fast switching. But, the minimum of \( V_{TH} \) is mainly limited by circuit functionality and noise margin [5]. Basically, \( V_{TH} \) is given by \( \log_{10}(I_{on}/I_{off}) \times S \). With DIBL taken into consideration, the \( I_{off} \) is measured at \( V_D=V_{DD} \). For SOI, with its nearly ideal subthreshold slope, offers the lowest \( V_{TH} \) for low power supplies. However, in PD SOI, \( V_{TH} \) depends on the SOI thickness, so that non-uniformity in the Si film increases the variation of \( V_{TH} \) across the wafer. PD SOI solves the above issue, but the neutral body not only causes the I-V kink and the transient effects, but also significantly increases \( I_{off} \) due to the worse DIBL.

3.2 Power dissipation

There are three major sources of power dissipation in CMOS digital circuits: switching power, short-circuit dissipation, and the leakage component. Thus, the total power dissipation can be described in the following [6],

\[
P_{TOT} = P_I(C_L \cdot V_{DD} \cdot f_C) + I_{sc} \cdot V_{DD} + I_{leak} \cdot V_{DD},
\]

where \( P_I \) is the activity factor, \( f_C \) is the clock frequency, \( I_{sc} \) is the short circuit current, and \( I_{leak} \) is the leakage current. Since SOI has lower parasitic capacitances and better subthreshold swing, it is expected that SOI circuits can be operated at lower supply voltages and also provide lower power dissipation.

4. Potential race problem in SOI switching circuits

4.1 Transient effect: clock dependence of chain delay

It has been reported that the propagation delay of non fully depleted floating body SOI inverter chains has a switching-history dependence: reducing the off-time of the switching clock leads to slower switching and the instability which is defined as \( t(\text{short})/t(\text{DC}) \) varies from 2% to 25% [7, 8, 9]. Here, the bi-stable body voltage states model was proposed, including reducing threshold voltage and
current overshoot. In addition, circuit simulation and inverter analysis with bi-stable states show the a similar trend as experimental results.

Body voltage, which can give both benefits and drawbacks to circuit applications, is determined by the impact ionization and recombination currents under DC steady state conditions [2]. However, in switching circuits, it is also affected by the extra impact ionization current \(I_{\text{imp}}\) and current overshoot due to dynamic capacitive coupling as shown schematically in Fig. 2. As a result, a switching history dependence of the body voltage with bi-stable states was proposed: in one state, the steady state, the body voltage reaches its DC level. The other, the quasi-state, is determined by DC current sources such as the extra impact ionization current and the “off” time of the clock. Using the nMOS in the inverter chain as an example, four different switching cases are considered as illustrated schematically in Fig. 3. In a single pulse or slow switching case, excess \(I_{\text{imp}}\) can be dissipated through recombination during the long “off” time and speed is determined by DC body effect and current overshoot during the switching. In the fast switching case, the excess \(I_{\text{imp}}\) charges up the body to reach a quasi-state due to the finite recombination rate and shorter “off” time. In fast switching region, the speed is determined by two competing effects: a speed-up effect due to the threshold voltage reduction as the body voltage increases, and a slow-down effect due to the loss of current overshoot. Finally, if circuits go through a long “off” time, excess components are dissipated through recombination and the body voltage returns to the steady state value.

In order to explain the speed degradation in fast switching, the role of the body voltage on the current overshoot has to be explored. In steady state or slow switching, as the gate switches from low to high, the body voltage is pulled above the \(V_{\text{body(steady state)}}\) at \((V_{DS}, V_G) = (\text{low, high})\). Then, source/body (SB) junction turns on to discharge the body back to its steady state value. As a result, the body voltage overshoot causes the drain current overshoot. On the other hand, during fast switching, the body voltage has already been charged to a high quasi-state with the SB junction turned-on, even before the gate switches from low to high. The resultant high quasi-state SB junction leakage reduces the overshoot during switching. In other word, the larger the difference between the body voltage before the switching and after, the greater will be the current overshoot, which enhances the speed. Thus, the inverter chain delay time model in Eq. (2) has to add an extra term, \(\tau(V_{DS}, T_{\text{off}})\), to include the current overshoot,

\[
\tau_D = \frac{1}{2} \left( \frac{1}{L_{DD}} \right) t_T + C_L \frac{V_{DD}}{2I_D} - \tau(V_{DS}, T_{\text{off}}),
\]

(3)

In the fast switching case, the body voltage shifts toward the quasi-state and the overshoot of the body voltage during switching is reduced, resulting in a smaller current overshoot. As a result, a slower switching speed is expected. In

Hspice simulation, a two-pulse signal with varied \(T_{\text{off}}\) was applied at the 7-stage inverter chains’ input where the body voltages of each transistor were set at their respective quasi-states. The simulation results (Fig. 4) show a trend similar to the experimental result [8].

4.2 Impact and solutions

As supply voltages are reduced, drain current overshoot becomes more important and a greater variation in circuit speed is observed [8]. Therefore, it is expected that there will be a more severe race problem in low supply voltage applications. Also, in fast switching applications, power dissipation is slightly larger than expected. This is due to the increased leakage current as the body voltage shifts from a lower steady state to a higher quasi-state as shown in Fig. 1. On the other hand, the increase of the source/body junction leakage current in the quasi-state leads to a smaller variation in speed as shown in Fig. 5. This suggests that the suppression of the floating body effect can reduce the frequency instability.

5. Trade-off among Body-tied, FD and PD SOI

Partially-depleted SOI MOSFETs with thick films are inherently immune to threshold voltage variation due to non-uniformity in film thickness, but suffer a degradation of the subthreshold slope and severe floating body effects, resulting in transient and kink effects in both saturation and subthreshold regions. Even though the halo between source and body can suppress these floating body effects [3], in mixed-mode circuits, these effects can still either increase the mismatch or reduce the output resistance.

Ideal body-tied SOI MOSFETs can completely suppress the floating body effect. However, some of body-tied structures, such as H-gate and Source/Body-tied SOI [1], not only increase device area, but also increase total gate oxide capacitances which can reduce speed. Furthermore, real body-tied devices suffer parasitic effects from the body contact and lose the floating body enhanced transconductance. In addition, there is another trade-off between body-tied Near-fully-depleted and body-tied PD SOI devices in terms of the effective body resistance and the subthreshold swing. A large effective body resistance can cause floating body effects [11] in wide devices, which limits the maximum device width as a basic unit.

For Fully-depleted SOI, the floating body effects still exist in these devices but are much weaker. However, the challenge for FD devices has been the control of \(V_{TH}\) and salicidation in the thin film. As these two issues have been solved [12], FD SOI will be a better candidate for future digital applications. Thus, in mixed-mode circuits, dual threshold voltage thin film SOI MOSFETs will be an optimal solution. The lower threshold voltage forms the PD SOI devices for the digital part and the higher threshold voltage forms the FD SOI devices with body contacts for the analog part.
6. Conclusion

In this paper, the physical mechanisms behind the clock dependence of inverter chain delay, which gets worse at low supply voltages, has been proposed. For low voltage applications, larger timing margins are required for the circuit designer to avoid the logic error due to the floating body induced frequency instability. However, this would effectively cancel out the inherent speed advantage provided by SOI. Consequently, the better solution is to suppress the floating body effect through either the design of source/body junction or the choice of device style.

Acknowledgment

This work was supported by Semiconductor Research Corporation. The authors would like to thank Dr. Klass Bult for help in circuit evaluation.

References


Unloaded 7-stage Inverter Chain 3rd stage delay time vs. Supply voltage Power dissipation vs. Supply Voltage

Figure 1. (a) Unloaded 7-stage inverter chain used in the Hspice simulation. (b) Simulated delay time versus supply voltage for both SOI and bulk CMOS inverter chains. (c) Simulated power dissipation versus supply voltage for both cases.
Figure 2. (a) Schematic plot of extra impact ionization current due to switching. (b) Schematic plot of the current overshoot due to capacitive coupling. (c) Formation of bi-stable body voltage states due to the extra impact ionization current charging effect.

Figure 3. Transitions between steady state and quasi-state for four switching cases: Inverter chain (1) starts fast switching, (2) maintains fast switching mode, (3) idles for a long “off” time, and (4) maintains slow switching mode.

Figure 4. Simulated third stage falling edge delay time measured at 2nd pulse for different “off” time, $T_{off}$.

Figure 5. The Normalized delay time versus $T_{off}$ for different source/body junction leakage currents.